CAVIAR Hardware Interface Standards, Version 2.0, Deliverable D_WP7.1b

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Abstract

The aim of this document is to define consortium hardware interface standards for the CAVIAR project to the extent that ensures the compatibility of all participants' devices, e.g. AER-PCBs, AER-chips, and AER PCI cards. Discussions with the ALA/VLSI project are conducted to try to keep those standards consistent with this project too.

What's new?

The following definitions were added to the previous release 1.01 of this document:

- Pin out of the 100 pin AER chip standard for a PGA100 packaging in section 2.1 has replaced the description of the JLCC84 package previously used by partner UiO that had been included as a starting point for discussions.
- The specifications of a standard PCB currently under development that will hold this 100 pin AER chips can be found in section 3.

1 AER bus

This section defines the cable and connectors that are used for the AER bus. The specifications apply for connections between PCBs holding any AER-chip, AER mapping devices, and computer cards. In the tables that describe the signals and signal blocks the pin numbers are also given in Matlab-notation:

AER signal name	description	ATA standard	pin number
Reserved	available to extend standard	/RESET	1
AE[0:15]	AER data	DD[0:15]	17:-2:3, 4:2:18
GND		GND	2, 19, 22, 24, 26, 30, 40
/REQ	AER request	DMARQ	21
/ACK	AER acknowledge	/DMAACK	29
Key-pin, not present		Key-pin, not present	20
Reserved		/DIOW	23
Reserved		/DIOR	25
Reserved		IORDY	27
Reserved		SPSYNC:CSEL	28
Reserved		INTRQ	31
Reserved		/IOCS16	32
Reserved		DA1	33
Reserved		PDIAG	34
Reserved		DA0	35
Reserved		DA2	36
Reserved		/IDE_CS0	37
Reserved		/IDE_CS1	38
Reserved		/ACTIVE	39

Table 1: Signal description of 40 pin IDC connectors according to the consortium's AER bus standard and the corresponding pin names in the ATA/133 standard.

$< start >:< step >:< stop >$ or in case $< step >$ is 1: $< start >:< stop >$. Example: 72:-1:65 corresponds to 72, 71, 70, 69, 68, 67, 66, 65. The signal names are, however, also written directly beside the pins in the graphics of the plugs, footprints and chip-padframes.

1.1 ATA/133 cable and connector

It was considered an easy 'off the shelf' solution to use a cable and connector that are widely spread for fast digital signals. We decided to use the ATA/133 standard that uses a 40 pin IDC connector and a 80 line ribbon-cable. It is usually used for data transfer from hard disks in most commercial PCs. The data lines are inter-spaced by ground connected lines for decoupling. Thus the special connectors are distributing the ground pins to every second line in the ribbon cable. (For very short connections normal 40 conductor ribbon cables and IDC connectors may be used.) The signal blocks are described in table 1. The pin assignment in the physical plugs is depicted in figure 1.

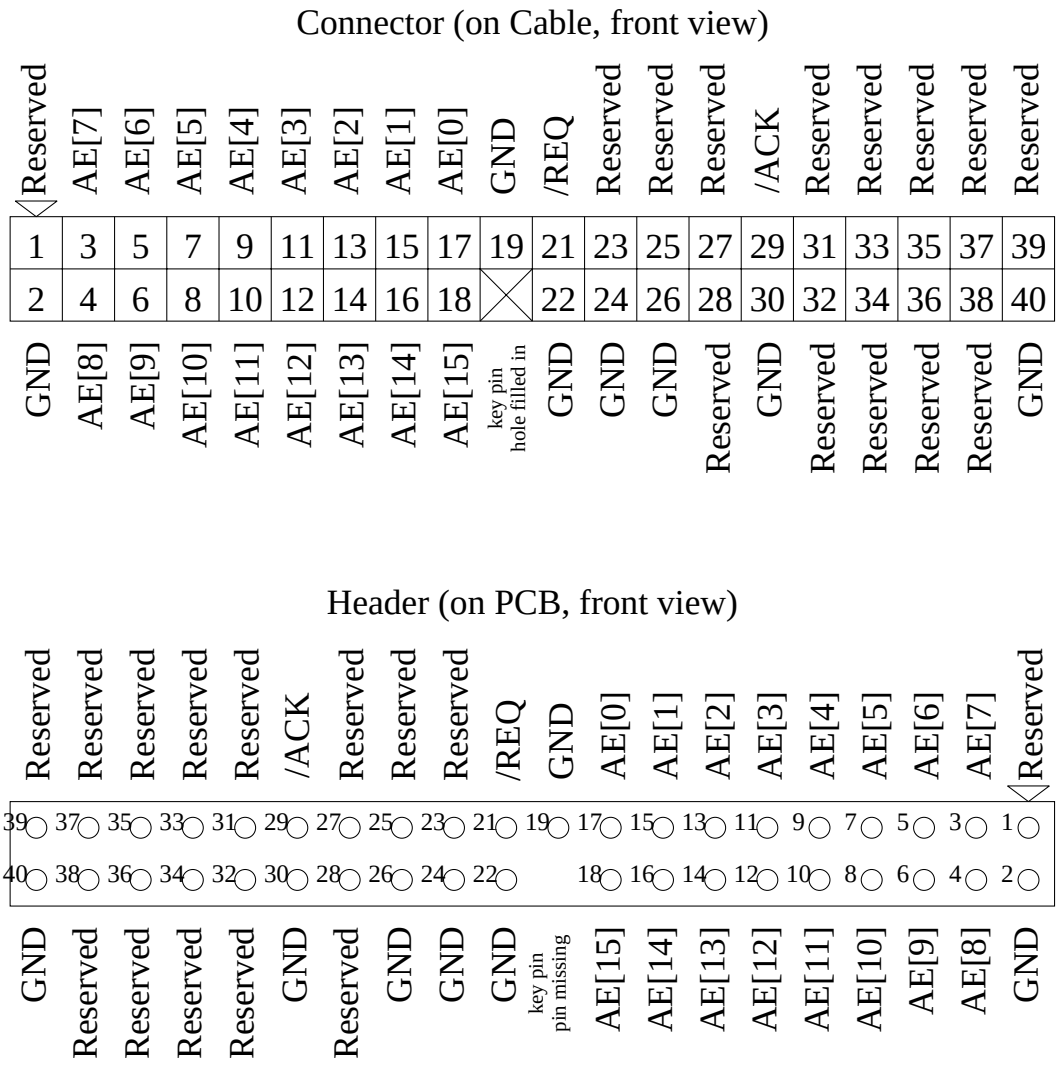

Figure 1: IDC 40 plugs for ATA/133 based AER bus standard

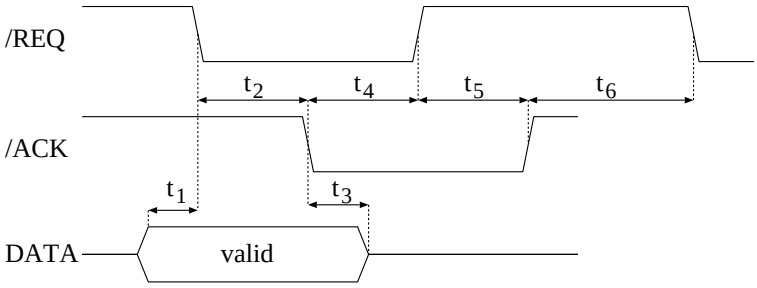

Figure 2: 4 phase handshake. Timing constraints in table 2.

	min	max	avg
t_1	0s	∞	
t_2	0s	∞	$\leq$ 700ns
t_3	0s	∞	
t_4	0s	100ns	
t_5	0s	100ns	
t_6	0s	∞	

Table 2: Timing requirements of 4 phase handshake (figure 2)

1.2 Protocol and Signal Timing

A single-sender/single-receiver scenario may be sufficient for most of the AER transmissions within the scope of this project. The AER remapper will have several inputs and outputs and can thus merge AEs from several senders and split them for several receivers. Where this is not sufficient, the consortium will decide on a multiple sender/receiver protocol. Candidate protocols are described later on in this section.

1.2.1 Single-sender/single-receiver

The asynchronous transmission protocol for the single-sender/single-receiver AEs will be a 4-phase handshake. The digital signal levels will be 5V (high) and 0V (low). Signal transition times should be below 10ns for the capacitive load of a bus cable, say typically well below 0.1nF. In other words the output current driving the transition (named short cut current in some data books) should be about 50mA. The usual causal rules for /REQ, /ACK and DATA (this is the address in AER) apply (figure 2). The causal order of the signals has to be maintained, i.e. all times in the figure need to be bigger than 0 (table 2). /REQ and /ACK are active low.

The upper time limits result from assumptions that determine the necessary bus bandwidth as follows: The biggest address space is the one used by the

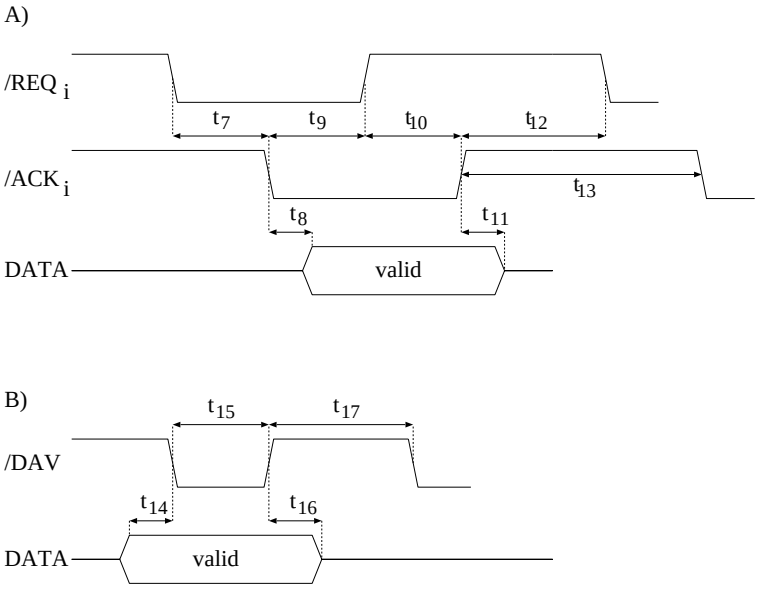

Figure 3: Bus protocols that have been used if several senders (A) or several receivers (B) share the DATA lines (the address-lines in AER). Timing constraints in table 3.

retina/imager chip, which might achieve a resolution of up to 128x128 pixels. That would correspond to a 14 bit address space, i.e. 16384 addresses. If we limit the firing frequency range for a pixel to maximal 100Hz and if we assume that never more than half the pixels will be active, then we can conclude that an AER bus needs to transmit never more than 819200 events per second. Thus one transmission can be allowed to last up to approximately 1μs. The timing requirements for t_4 and t_5 in table 2 ensure that a transmission lasts but 200ns once both partners have agreed to transmit. It is very desirable that our devices will be even faster than those upper limits. The avg requirement for t_2 ensures that the average total transmission time is below 900ns. The receiver is however allowed to put the sender on hold longer than that in individual cases. This might be unavoidable for some time when the receiver is an AER remapper that merges several inputs. All other devices should aim at having this delay shorter than 100ns.

1.2.2 Multiple-sender/Multiple-receiver

We also include two protocols in this document where multiple sender or multiple receiver share the DATA lines (figure 3 and table 3). They have been used previously by partner ETHZ. The time limits valid for the circuits used then are given in table 3. These time limits will however be adapted for our specific needs

	min	max
t_7	0	∞
t_8	0	75ns
t_9	0	175ns
t_{10}	0	225ns
$t_9 + t_{10}$	225ns	∞
t_{11}	0	100ns
t_{12}	0	∞
t_{13}	100ns	∞
t_{14}	0	∞
t_{15}	190ns	260ns
t_{16}	0	∞
t_{17}	0	∞

Table 3: Timing requirements of protocols in figure 3.

in any case, if we decide to use these protocols. Using these protocols might become necessary to merge larger numbers of AE-senders or to send to larger numbers of AE-receivers than there is AER connectors on the AE mapping device. This will have to be decided upon in the course of the project.

Figure 3 A) shows a protocol that has been used when several AER chips send to one receiver that is controlling the bus. There is a pair of control lines for a request and an acknowledge signal for every sender. The request is controlled by the sender and the acknowledge by the receiver. The acknowledge is used to grant bus access and the data has to be supplied by the sender i within a minimal delay after /ACK$_i$ has been applied (see table 3).

Figure 3 B) describes a protocol where the data lines are shared by several receivers. The only control line is for a data valid signal controlled by the single sender.

2 AER chip pin-out

Chips that follow the pin-out specifications in this section will fit into a standard AER PCB (see section 3) that can be shared by the partners. Chips that do not follow these specs require the design of an extra PCB that needs to comply with the connector standards for the AER bus (section 1).

2.1 100 pin PGA package

Discussions within the consortium indicated that a 100 pin packaging is desirable. The most likely candidate was a 100 pin PGA package. A through hole chip socket would also allow lenses to be mounted on the socket. However, it might be a better idea anyway to design lens-mounts that are fixed to the PCB.

signal name	description	pin number
CDGND	core digital supply GND	1
CDSUBS	core digital substrate GND	2
C[0:19]	'control' pins for additional chip specific signals	3:11,14:24
AGND	analog supply GND	12,37
AVDD	analog supply VDD	13,38
ASUBS	analog p-bulk GND	25
AWELL	analog n-bulk VDD	26
A[0:19]	analog pins for biases and/or probes	27:36,39:48
IPU	pull-up bias for wired NOR used in AER receiver	49
IPD	pull-down bias for wired NAND used in AER receiver	50
OPU	pull-up bias for wired NOR used in AER sender	51
OPD	pull-down bias for wired NAND used in AER sender	52
O[0:15]	output AER data lines	60:-1:53,91:98
PDSUBS	peripheral digital p-bulk GND	61,89
PDGND	peripheral digital supply GND	62,87
PDVDD	peripheral digital supply VDD	63,88
PDWELL	peripheral digital n-bulk VDD	64,90
I[0:15]	input AER data lines	72:-1:65,79:86
/IACK	input AER acknowledge	73
/IREQ	input AER request	74
DPADVDD	pad supply and n-bulk VDD	75
DPADGND	pad supply and p-bulk GND	76
/OREQ	output AER request	77
/OACK	output AER acknowledge	78
CDWELL	core digital n-bulk VDD	99
CDVDD	core digital supply VDD	100

Table 4: Signal description for the PGA100 package.

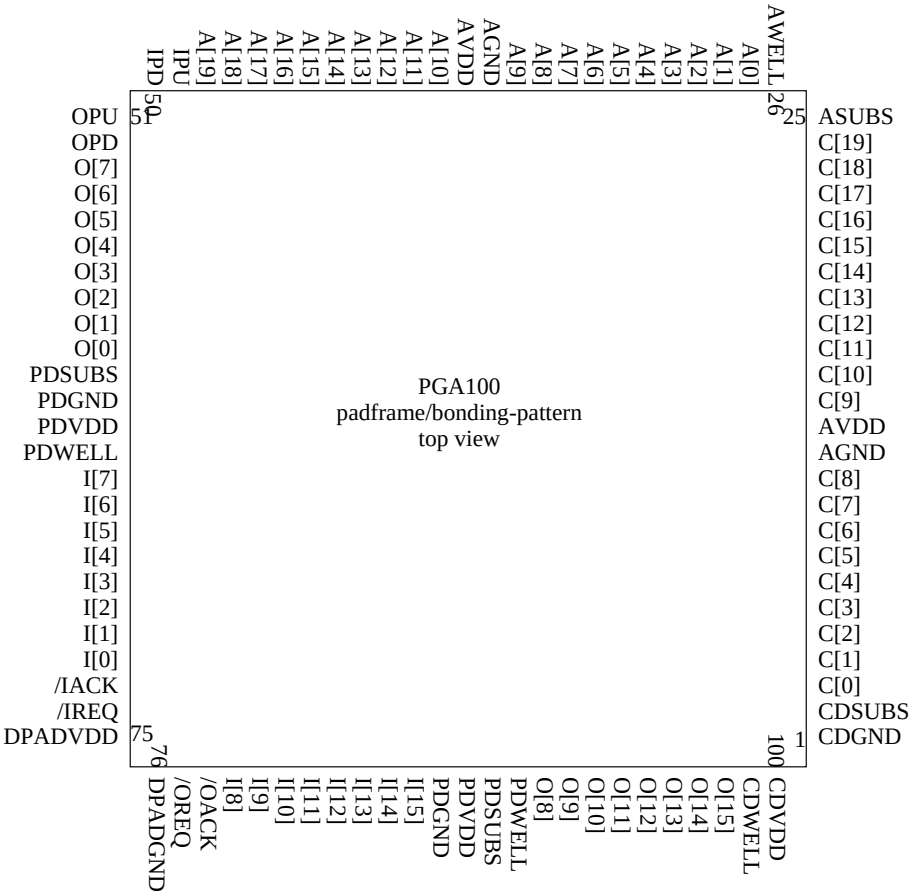

Figure 4: The bonding of the signals to the boarder of the PGA100 package cavity. This normally corresponds to the arrangement of the signals on the chip padframe too.

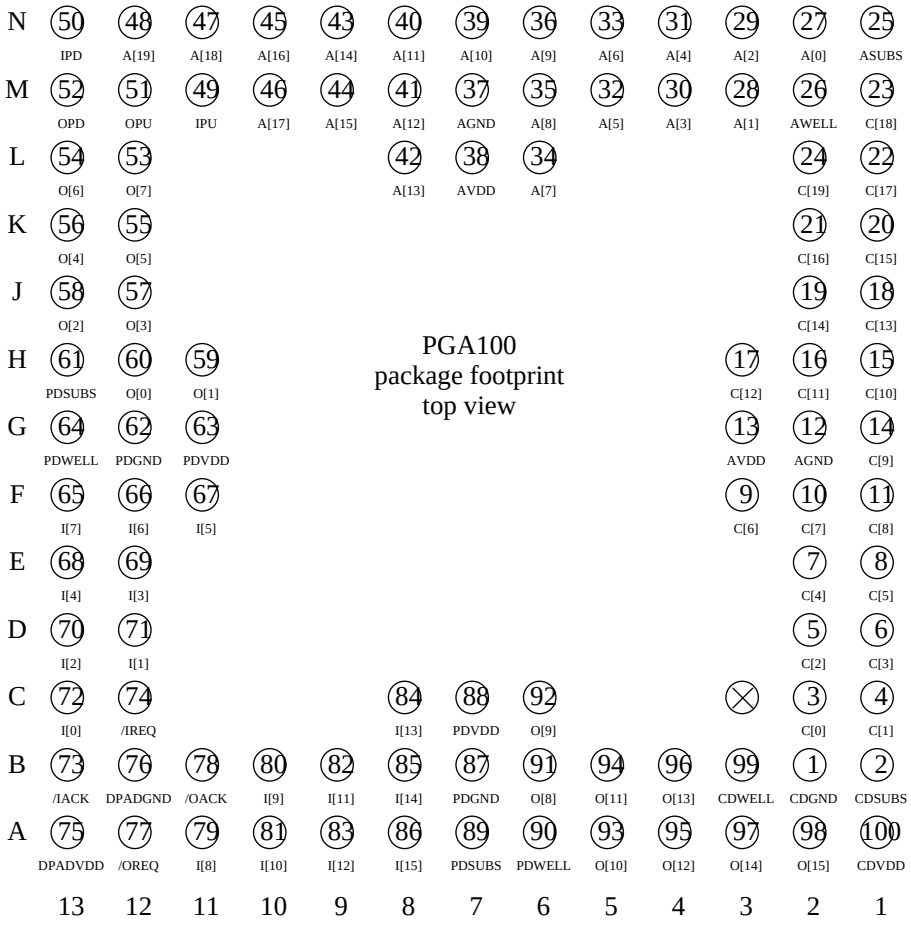

Figure 5: The PGA100 footprint with signal names.

The major concern with PGA packages and through hole mounting was that of high speed. Different cable lengths inside the package may cause different delays and through hole mounting will add extra capacitance. The fact that Pentium chips can be found in PGA packages (although surface mount) indicated however, that some of these limitations could be overcome by assigning the pins carefully.

We finally decided to go for the 100 pin PGA as the best compromise. The different signals are described in table 4. The pin assignment for the bonding and for the footprint is depicted in figures 4 and 5. It was decided to use four basic signal blocks: AER input (I[0:15],/IREQ,/IACK), AER output (O[0:15],/OREQ,/OACK), a block usually used to supply analog biases to the chip (A[0:19],IPU,IPD,OPU,OPD), and a block to supply additional (usually digital) control or data signals (C[0:19]). The major consideration in assigning them to the padframe was that of keeping analog and digital signals well separated. There are also 7 separate vdd/vss pairs available from the padframe: The pad power supply (DPADVDD/GND), peripheral digital circuit (PDVDD/GND) and bulk supply (PDWELL/SUBS) primarily for the AER communication logic, core digital circuit (CDVDD/GND) and bulk supply (CDWELL/SUBS), and analog circuit (AVDD/GND) and bulk supply (AWELL/SUBS).

3 AER PCB

Partner UiO is at present working on a standard PCB to host AER chips that conform to the specifications in section 2. The layout of a first version that is in production can be seen in figure 6. A component list for that board can be found in appendix A. The following features are included:

- 4 IDC40 connectors for the four signal blocks.

  The AER input and output block are assigned to the header following the specs in section 1. The other two (figures 7 and 8) use the same pins for signals plus a few more in addition. They can thus optionally be used as additional AER connectors for specific chips. An array of Schottky diodes is included to terminate the address event input lines I[0:15] and the signals /IREQ and /OACK.

- 24 on-board voltage sources.

  The voltage sources are potentiometers. Their output is stabilized with capacitors to GND and AVDD and buffered by followers. The 24 analog signal lines can be connected individually either to their pin in the IDC40 header for external voltage sources or to one of these on-board voltage sources. Partner ETHZ is currently developing a computer controlled DAC board as a source for external voltages. With this DAC board it will be easy to automatically test different analog parameter voltage configurations. The on-board voltage sources can be connected once the parameter configuration remains fixed.

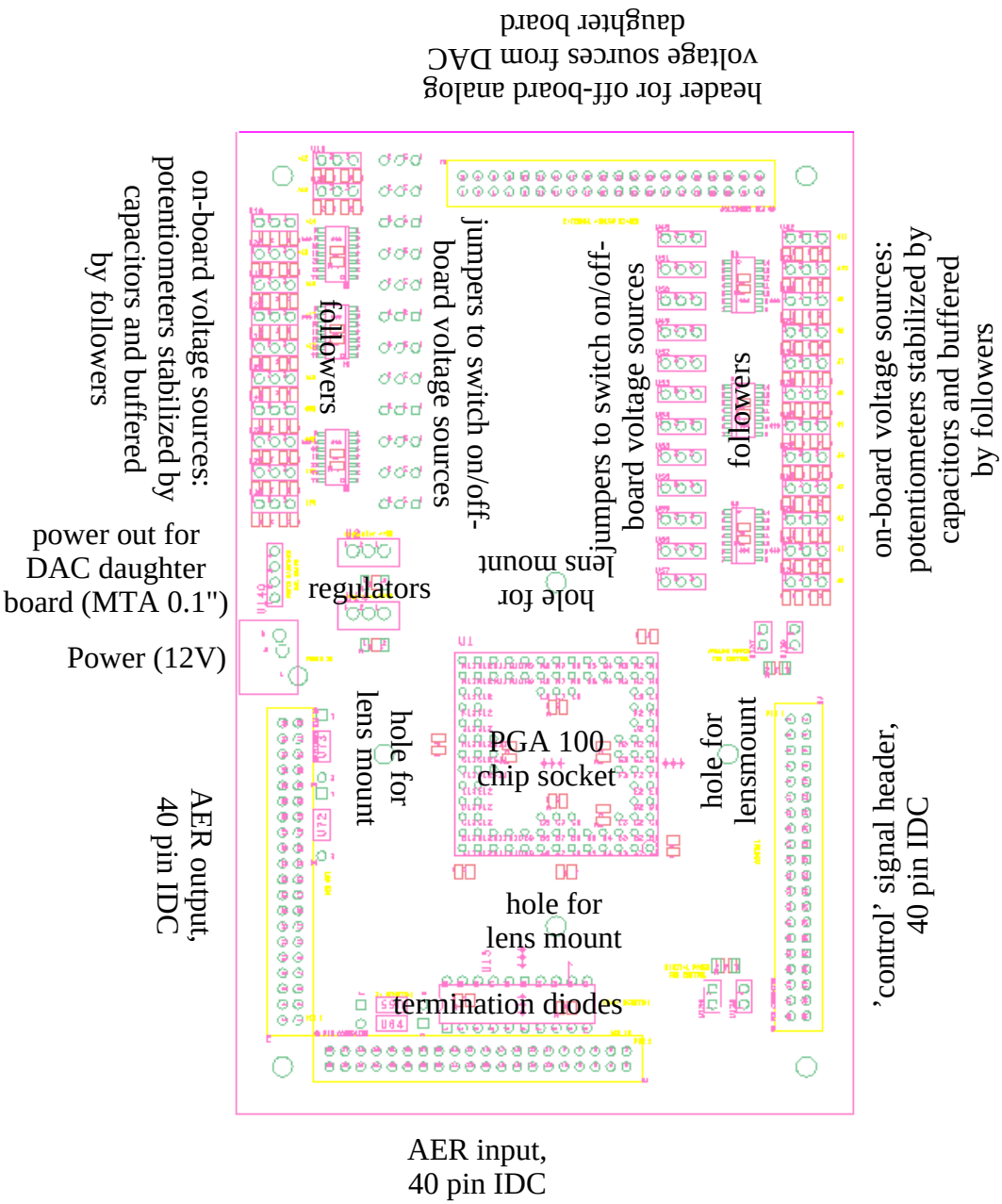

Figure 6: The AER-PCB prototype

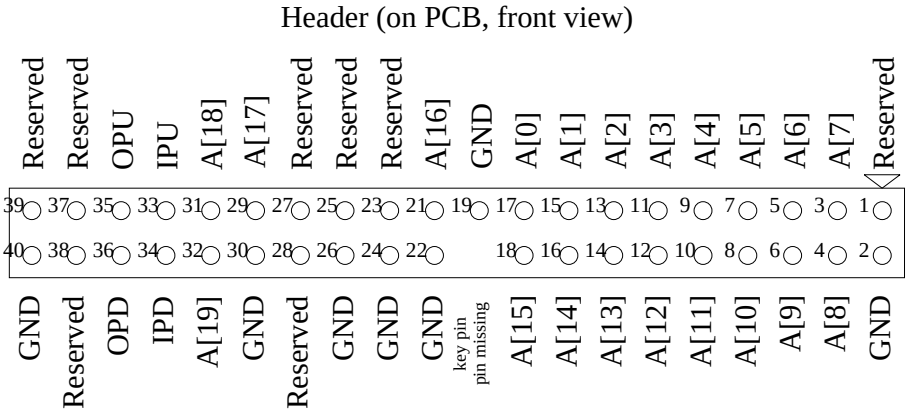

Figure 7: The IDC40 header on the PCB for the analog signal block

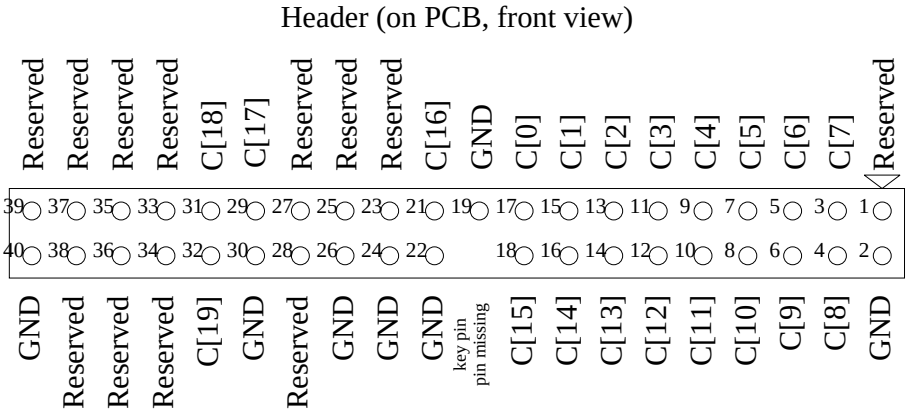

Figure 8: The IDC40 header on the PCB for the control signal block

- 12V power input plus two regulators for digital and analog 5V power supply.

  A 12 V power plug supplies two regulators that power two pairs of power planes on th PCB, AVDD/GND and DVDD/GND. The control signal block will have its own power plane pair that can be connected to either AVDD/GND or DVDD/GND. This is because the control signals can optionally also be used for analog signals. An additional connector will convey the unregulated 12V power supply lines and the analog power voltages to the DAC board.

A Component List for the Generic AER Board

Part description	Footprint	Quant.	Brand	Part no.	Distrib.	order number
2x16 Schottky diodes for bus termination	20-DIP	1	TI	SN74S1053N	Farnell	149-0709
EQUIVALENT:						
2x16 Schottky diodes for bus termination	20-DIP	1	TI	SN74S1053N	Newark	52F2684
IDC 40 headers	2x20 0.1" pitch	4	Harting	09185407323	Farnell	302-1385
500kΩ Potentiometers	3 pin 0.1" pitch	24	?	?	ELFA	64-744-64
EQUIVALENT:						
500kΩ Potentiometers	3 pin 0.1" pitch	24	Bourns	3296W-1 500K	Farnell	347-917
Quad OpAmp	SMD	6	NS	LM6144BIM	ELFA	73-113-68
EQUIVALENT:						
Quad OpAmp	SMD	6	NS	LM6144BIM	Farnell	554-111
5V regulator	TO-220	2	ST	LD1086V50	Farnell	352-9897
4 pin 0.1" pitch MTA connection header	4 pin 0.1" pitch	1		640457-4	Farnell	588-738
4 pin 0.1" pitch MTA housing for 24AWG cables	not applicable	1		640441-4	Farnell	588-179
SMD Capacitor 0.1μF ceramic X7R	0805	20			ELFA	65-766-31
SMD Capacitor 1nF ceramic NP0	0805	20			ELFA	65-763-42
EQUIVALENT:						
SMD Capacitor 1nF ceramic NP0	0805	20	AVX	08055A102J-MR	Farnell	355-4594
SMD Capacitor 10μF tantal	B 3528	2			Farnell	331-3890
Power-Header		1	LUTRONIC	NEB/J21RL	Farnell	838-858
Power-Plug Housing		1	LUTRONIC	NES/J21RL	Farnell	838-780