

AER Building Blocks for Multi-Layer Multi-Chip Neuromorphic Vision Systems

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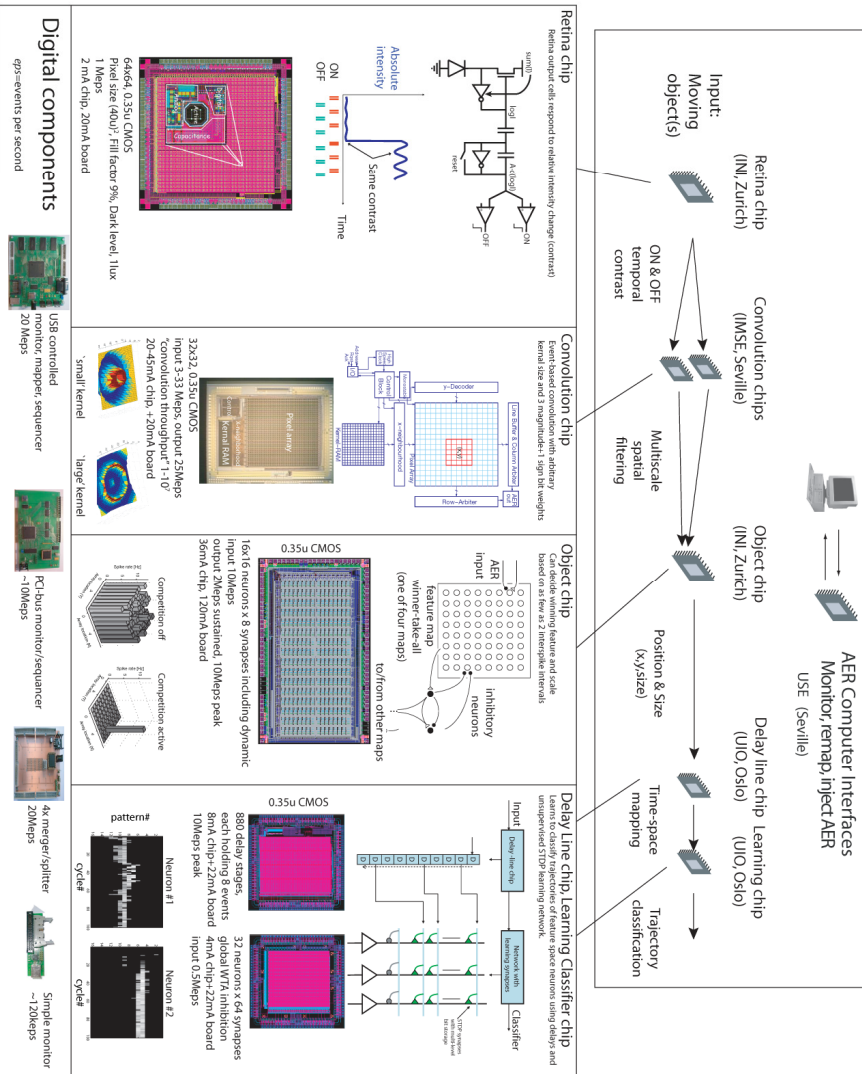
USE: University of Seville

Anton Ciri, I. Garcia-Vargas, F. Gomez-Rodriguez, G. Jimenez, A.

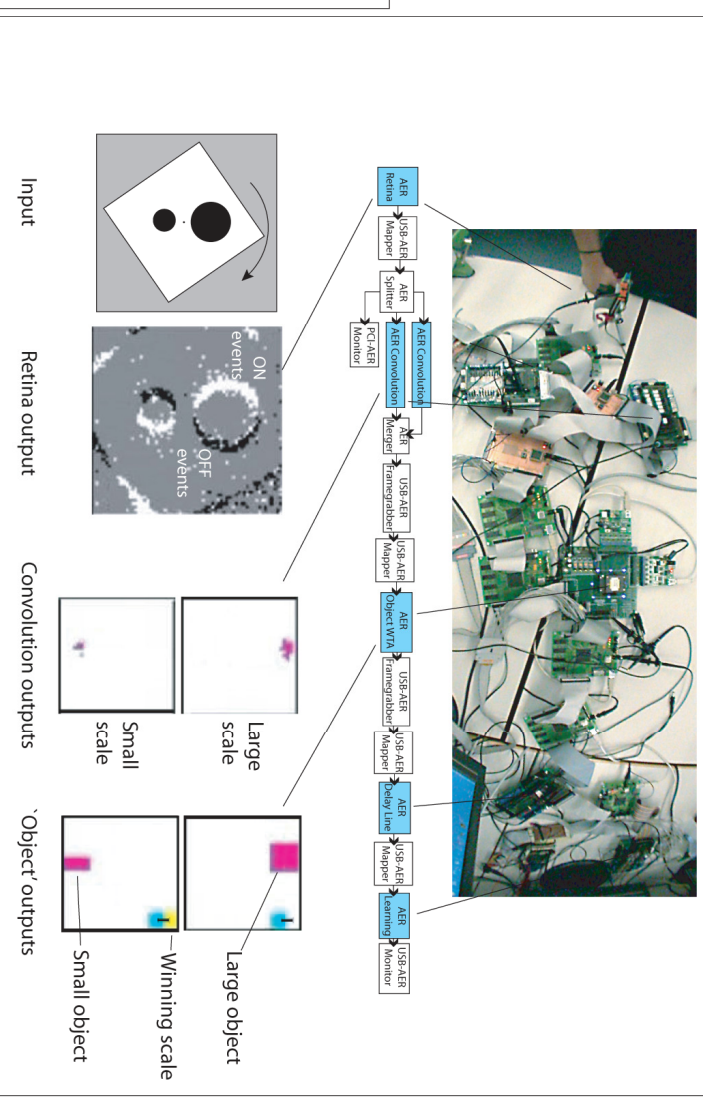
Linares-Barranco, L. Miro, R. Paz, M.A. Rodriguez, R. Senhadji-Havarró

We report progress in the construction and characterization of an event-based hardware vision system (CAVIAR) that learns to classify spatio-temporal trajectories.

CAVIAR components use the Address-Event Representation (AER) for communication. The identities of spiking neurons are communicated asynchronously on shared digital buses.



Our characterization so far showed that stimuli of two different shapes on a rotating disk could simultaneously be discriminated and their position extracted at level of the object chip.



CAVIAR is the largest AER system yet assembled. It is a step towards efficient architectures for data-driven adaptive real time vision systems.

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Digital components

995+events per second



USB controlled monitor/mapper sequencer
20 Mbps



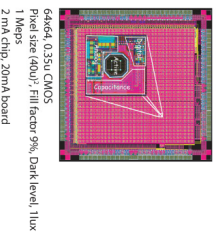
FC-Cluster monitor/sequencer
100Mbps



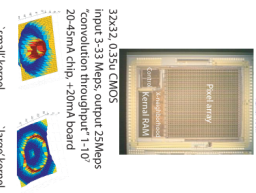
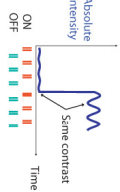
4x merger/splitter
20Mbps



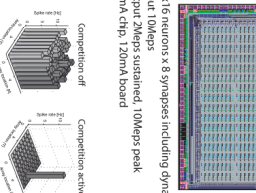
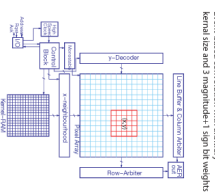
Simple monitor
~120kpps



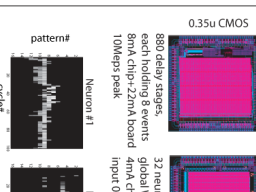
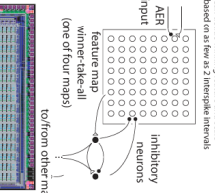
64x64 0.35u CMOS
Pixel size (40u); Fill factor 9%, Dark level: 1lux
1 Mbps
2 ma; chip, 20ma board



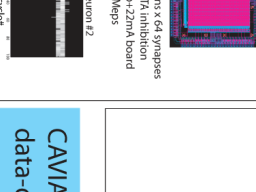
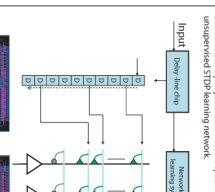
32x32 0.35u CMOS
Input: 3.33 Mbps, output: 25Mbps
"convolution-throughput" ~1-10^7
20-45ma chip, +20ma board



0.35u CMOS
16x16 neurons x 8 synapses including dynamic
input: 10Mbps
output: 2Mbps sustained, 10Mbps peak
36ma chip, 120ma board



0.35u CMOS
880 delay stages
each holding 8 events
8ma chip-22ma board
10Mbps peak



32 neurons 1.6k synapses
each holding 8 events
47ma chip-22ma board
input: 0.5Mbps

