IMSE -cnm Instituto de Microelectrónica de Sevilla

ANNUAL REPORT 2024

IMSE-cnm Instituto de Microelectrónica de Sevilla

CSIC Consejo Superior de Investigaciones Científicas

Universidad de Sevilla

INSTITUTO DE MICROELECTRÓNICA DE SEVILLA
Centro Nacional de Microelectrónica

C/ Américo Vespucio
(Intersection with Leonardo Da Vinci)
PCT Cartuja: 41092 - Seville, Spain

Phone: +34 95 446 66 66
Fax: +34 95 446 66 00

www.imse-cnm.csic.es

Layour and design: tiporium.com

OUTLINE

FOREWORD

Teresa Serrano Gotarredona

This report summarizes the research activities and the main achieved objectives by the Instituto de Microelectrónica de Sevilla (IMSE) during 2024

It is my pleasure to present IMSE's 2024 Annual Report, highlighting a year of remarkable achievements, international collaborations, and scientific excellence. Our institute has continued to strengthen its position as a leading research center in microelectronics, combining world-class scientific output with a strong commitment to innovation, industry, and society.

In May 2024, IMSE was honored with the Aspira-MaX Josefa Barba Excellence Seal and joined the **Deep-MaX-CSIC Excellence Program pathway**. The goal of this program is to position IMSE as an international benchmark in the microelectronics sector by increasing the impact of its scientific output, strengthening participation in internationally funded collaborative programs, and enhancing technology transfer to both industry and society.

In line with this strategic roadmap, IMSE maintained a strong presence in international research initiatives throughout the year. A total of **13 collaborative EU projects** were active in diverse fields such as defense applications, cybersecurity, and neuromorphic engineering.

At the national level, IMSE took part in over **25 competitive research projects** in collaboration with Spanish universities and companies.

The institute's scientific output in 2024 included **82 Scopus-indexed publications**, notably a paper in Nature Communications resulting from a collaboration with IBM Zurich, as well as a study on meteorological observation in Uranus—conducted with INTA, the University of Oxford, and the University of Reims—published in Space Science Reviews.

During the same year, IMSE filed **three new patent applications** and executed **11 industrial contracts**, further reinforcing its commitment to innovation and technology transfer.

Outreach and social engagement also remained a priority, with IMSE participating in **European Researchers' Night**, the S**eville Science Fair**, and hosting numerous public and school visits as part of its educational activities.

Overall, 2**024 was a year of intense research activity, international collaboration, and outstanding scientific productivity** for IMSE.

DIRECTIONS:

The Instituto de Microelectrónica de Sevilla (IMSE) is located in the Parque Científico y Tecnológico Cartuja (Cartuja Scientific and Technological Park) on Isla de La Cartuja, at the corner of Calle Américo Vespucio and Calle Leonardo da Vinci.

C/ Américo Vespucio, 28. Parque Científico y Tecnológico Cartuja – 41092 Sevilla, Spain

+ 34 954 466 666

www.imse-cnm.csic.es

info@imse-cnm.csic.es

GPS: 37° 24' 44" N - 06° 00' 21" W

ABOUT IMSE

The Instituto de Microelectrónica de Sevilla (IMSEC-NM - Seville Institute of Microelectronics) is an R&D&I joint center of the Consejo Superior de Investigaciones Científicas (CSIC - Spanish National Research Council) and the Universidad de Sevilla. Together with its counterpart institutes in Barcelona and Madrid, it forms part of the Centro Nacional de Microelectrónica (CNM - National Microelectronics Center).

The Institute is dedicated to the field of Physical Science and Technologies, one of the eight areas into which research activity is divided by the CSIC. Its main area of specialization is the design of CMOS analog and mixed-signal integrated circuits and their use in different application contexts such as radiofrequency, microsystems or data conversion.

The IMSE-CNM began its operations in October 1989 under the auspices of an agreement signed by the Junta de Andalucía (the Andalusian Regional Government), the CSIC and the Universidad de Sevilla.

Its founding research group was initially based on the premises of the Centro de Informática Científica de Andalucía (CICA – Scientific Computing Center of Andalucía), as a subsidiary department of the Instituto de Microelectrónica de Barcelona (Barcelona Institute of Microelectronics).

Later, in 1996, it was established by the Governing Board of the CSIC as a Institute in Formation, occupying a building next to the CICA ceded by the Junta de Andalucía. In late 2008, the Institute was enlarged and relocated in new premises purpose-built by the CSIC in the Parque Científico y Tecnológico Cartuja (Cartuja Scientific and Technological Park).

On October 2015, by means of a Specific Collaboration Agreement signed by the CSIC and the Universidad de Sevilla, the center became a Joint Institute of both institutions.

The IMSE-CNM staff consists of approximately one hundred people, including scientists and support personnel. Most of them work for the CSIC and the Universidad de Sevilla. IMSE-CNM employees are involved in advancing scientific knowledge, designing high level scientific-technical solutions and in technology transfer. Their duties include both research and teaching activities, the latter mainly at official master and PhD degrees.

The projects undertaken at the Institute mostly correspond to EU research initiatives, National R+D Plans and Research Plans funded by the Junta de Andalucía. They focus primarily on implementing innovative concepts in silicon, using either the CNM's own clean room at the Instituto de Microelectrónica de Barcelona (IMB-CNM) or external foundries, mainly from Europractice or CMP IC services. The Institute also participates in several technology and knowledge transfer activities with microelectronics companies, at both national and international level.

These activities take the form of collaboration in numerous research contracts, the organization of training courses and the provision of scientific and technical consultation services for companies and government departments.The Instituto de Microelectrónica de Sevilla (IMSE-CNM) is a joint center of the Consejo Superior de Investigaciones Científicas (CSIC - Spanish National Research Council) and the Universidad de Sevilla.

ORGANIZATION

The Instituto de Microelectrónica de Sevilla (IMSE-CNM) is a joint center of the Consejo Superior de Investigaciones Científicas (CSIC - Spanish National Research Council) and the Universidad de Sevilla. The IMSE-CNM management structure is as follows:

Direction: Teresa Serrano Gotarredona
direccion.ims-cnm@csic.es

Vice-Direction: Diego Vázquez García de la Vega
dgarcia@imse-cnm.csic.es

Technical Vice-Direction: Joaquín Ceballos *Cáceres joaquin@imse-cnm.csic.es*

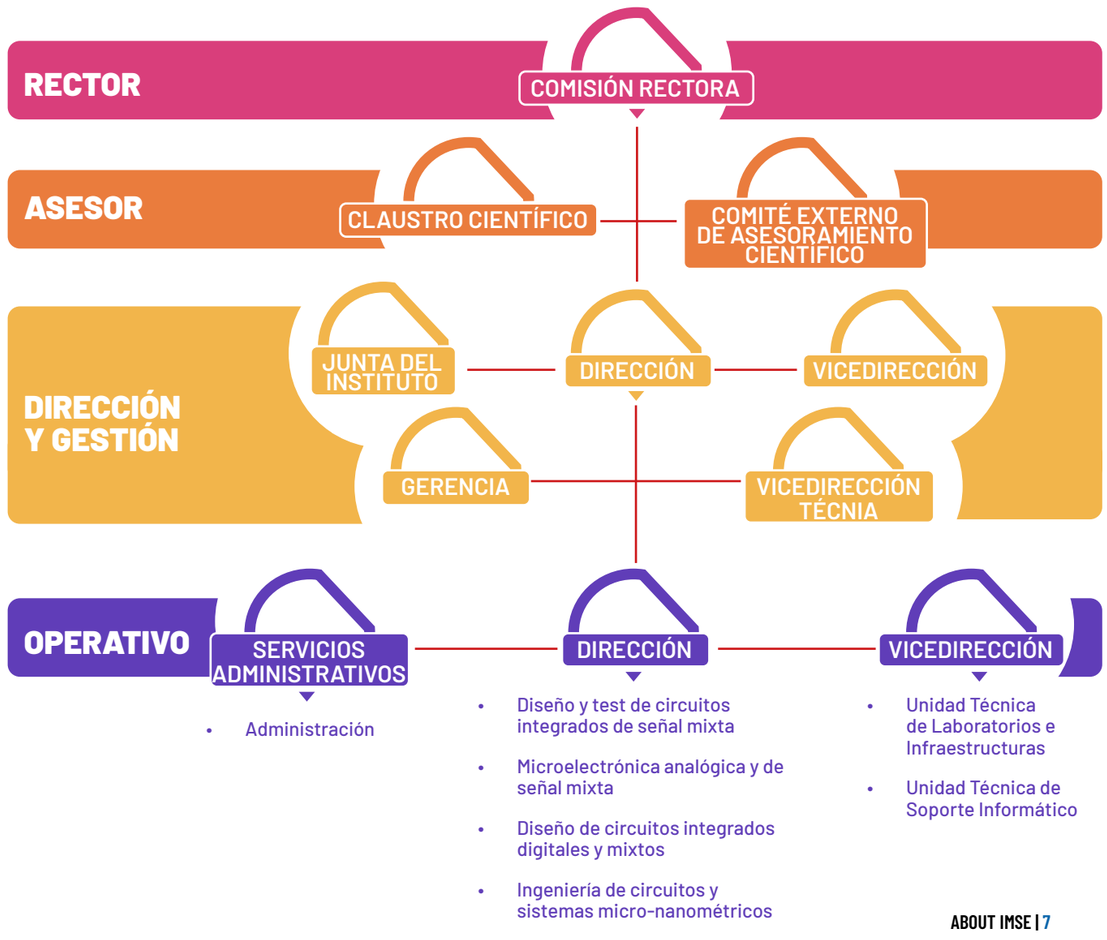
Management: José Francisco Barreña Moreno
gerencia.ims-cnm@csic.es

ADMINISTRATIVE SERVICES UNIT
The Institute's research activities are carried out by Research Units responsible for project development. There are currently four of these units, corresponding to different Junta de Andalucía TIC Groups:

- TIC 178: Design and Test of Mixed-Signal Integrated Circuits
- TIC 179: Analog and Mixed-Signal Microelectronics
- TIC 180: Design of Digital and Mixed-Signal Integrated Circuits
- TIC 026: Micro/Nanometric Circuits and Systems

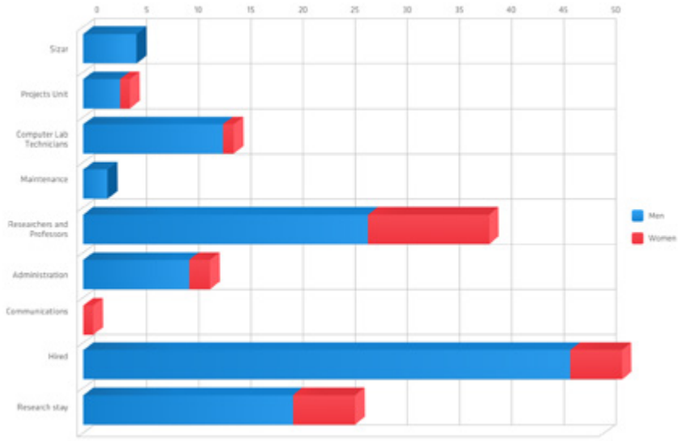
The Institute's infrastructure is also supported by two Technical Units.

- Laboratories and Infrastructures Technical Unit
- Computer Support Technical Unit



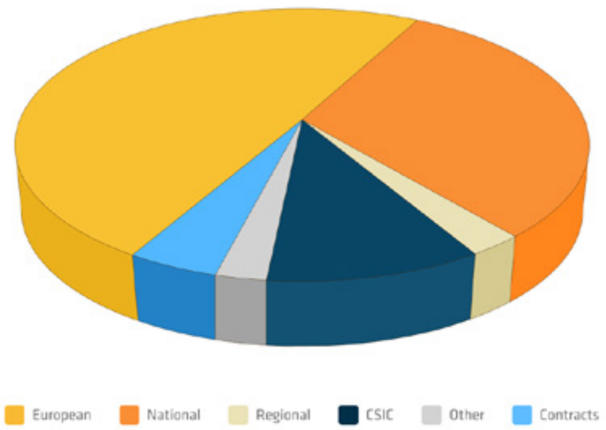
HUMAN RESOURCES

The personnel at the IMSE-CNM permanently or temporarily engaged in the Institute's activities includes nearly 123 people. Most of them work for the CSIC and the Universidad de Sevilla, but there are also teachers and students from other organisms on research internships as it is shown in the figure. These internships do not imply any kind of employer-employee relationship with the CSIC.



BUDGET

Incoming resources, distributed by concepts, for the year 2024 are shown in the following graphs (excluding staff costs). External funding is obtained either from competitive public projects or industrial contracts. Operating expenses are provided by CSIC and Universidad de Sevilla.



INFRASTRUCTURE

LABORATORIES

IMSE-CNM has its own laboratories and workshops, specifically habilitated for research, development and innovation tasks carried out at the Institute. The laboratories are well fitted out with equipment and instrumentation, and are run by a permanently employed team of specialists.

Head of Unit

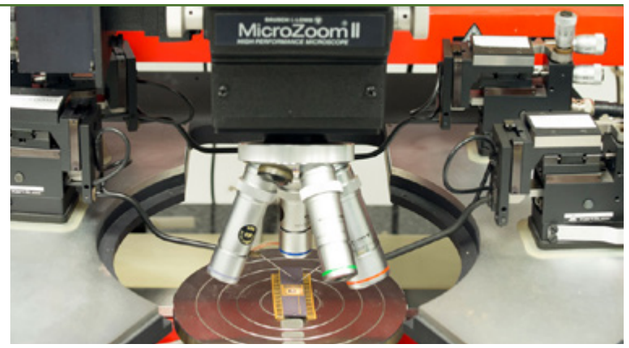
Joaquín Ceballos Cáceres
joaquin@imse-cnm.csic.es >

Device Characterization Lab

This laboratory is mainly dedicated to perform parametric measurements in semiconductors and passive devices. In this lab it is possible to acquire internal signals from the semiconductors, already cutted and packaged, or from wafers up to 3.5", and performing tests at temperatures ranging from -125ºC to 150ºC.

Chief Lab Technician

Antonio Ragel Morales
ragel@imse-cnm.csic.es



Equipment

Semiconductor Parameter Analyzers, Climatic Chambers, Probe Station, Temperature Forcing System, C Meter CV Plotter, LCR Meter.

Optoelectronics Lab

This lab is equipped with the instrumentation needed to characterize visible light sensors and integrated circuits made up of discrete sensors or visible light matrices. A dark chamber is also available for sensor characterization.

Chief Lab Technician

Antonio Ragel Morales
ragel@imse-cnm.csic.es

Equipment

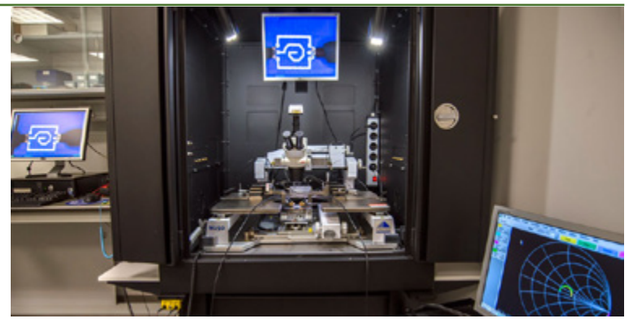
Optical Characterization Equipment, Monochromator, Pulsed Laser, Video Development Platform, Lux Meter, Laser Modules, Photo and Video Lenses, Spectrometer

Radiofrequency Lab

It alllows to perform spectrum and network measurements, and it is equipped with an anechoic chamber for device characterization or electromagnetic compatibility (EMC) measurements. It also allows to perform on wafer (up to 150 mm) as well as on printed circuit measurements.

Chief Lab Technician

Antonio Ragel Morales
ragel@imse-cnm.csic.es



Equipment

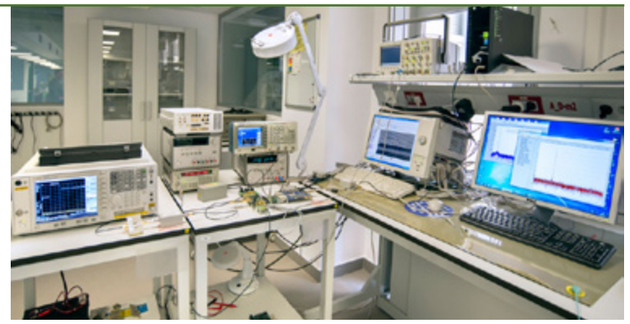
Anechoic Chamber, Noise Figure Analyzer, Spectrum/Network Analyzers, Probe Station, Vector Signal Generators, Noise Sources, Power Meter

A/D Measurement Lab

This is the largest lab in the IMSE. It has twelve fully-reconfigurable mobile stations to carry out the experimental tests on mixed-signal integrated circuits. It also has twelve carts with spectfic measurement equipment that can be attached to any of the mobile stations depending on the requirements of the A/D measurements to perform.

Chief Lab Technician

Antonio Ragel Morales
ragel@imse-cnm.csic.es



Equipment

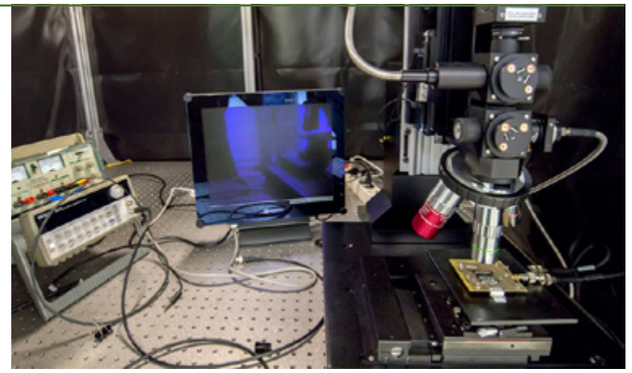
Spectrum/Network Analyzers, Logic Analyzers, Arbitrary Waveform Generators, Pulse Generators, Oscilloscopes, Data Acquisition Boards, Differential Amplifiers, Frecuency Counters, Switch/Control Unit, Test Systems, Power Meter, Electrometer, Lock-in Amplifier, Picoammeter, Phase Noise Measurement System.

Pulsed Laser Lab

This lab is equlpped with the new pulsed laser PULBOX PICO-RAD compact system for single-event effects testing. Using a single photon technique and a 1064nm wavelength (near-infrared) pulsed laser source, this facility allows the study of the impact of high energy particles over integrated circuits for space, medical or nuclear applications.

Chief Lab Technician

Antonio Ragel Morales
ragel@imse-cnm.csic.es



Equipment

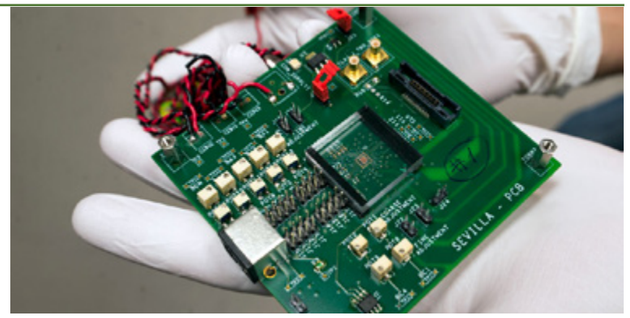
Pulsed Laser, Oscilloscope

Cibersecurity Lab

The Cibersecurity Laboratory has the required equipment to evaluate the immunity against different types of collateral channel attacks, which are based on the information obtained from the physical implementation of the cryptosystems (power consumption, algorithm's execution time, response to induced failures, electromagnetic emission, etc.).

Chief Lab Technician

Antonio Ragel Morales
ragel@imse-cnm.csic.es



Equipment

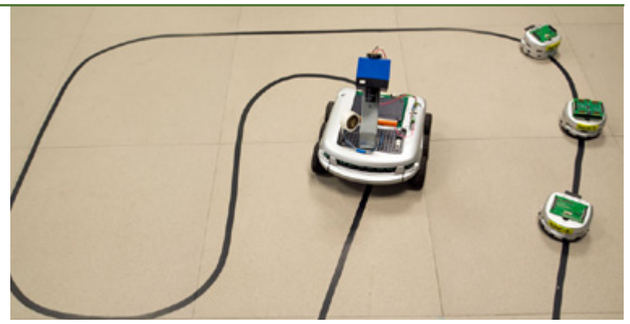
Device Current Waveform Analyzer, Logic Analyzers, Function Generators, Pulse Generators, Oscilloscopes, Arbitrary Waveform Generator, Power Meter, Motorized XY Microscope Stage, Ultra Wide Band Low Noise Amplifier, Data Acquisition System, Power Supply

Complex Systems Lab

This lab has been designed to provide accommodation to those systems that, due to either their size or their special characteristics, require a greater space or an isolated environment. It is also equipped with a showcase for the manipulation of dangerous chemical products and a security cabinet.

Chief Lab Technician

Antonio Ragel Morales
ragel@imse-cnm.csic.es



Equipment

Koala Robot, Area Preparation System, 3D Printer

ATE Agilent 93000

The Agilent 93000 SOC C200e Semiconductor Test System allows carrying out prototyping and fabrication tests of mixed-signal circuits (either already packaged or directly onto the wafer) in one only platform. It is also posslble to incorporate the Thermonics T-2650 BV, a temperature forcing system that allows to perform the tests under temperature conditions ranging from -55ºC to 200ºC.

Chief Lab Technician

José M. Mora Gutiérrez
jmiguel@imse-cnm.csic.es

Equipment

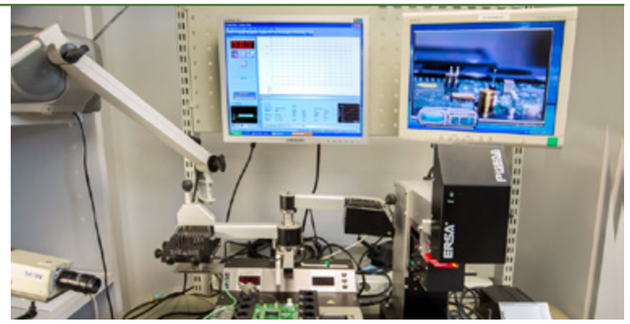
Agilent 93000 Semiconductor Test System, Temperature Forcing System, Oscilloscope

Special Assembly Workshop

The Special Assembly Workshop has equipment for soldering and desoldering high density packaging components, such as BGAs, mini-BGAs and fine-pitch surface-mount components.

Chief Lab Technician

Miguel A. Lagos Florido
mlagos@imse-cnm.csic.es



Equipment

IR Rework System, Precision Placement System, Soldering Stations

Packaging Workshop

This workshop is devoted to make the bonding between chip and package. It has all the required resources to face the challenges that deep-submicron technologies pose, allowing connections with pitch sizes down to 50 µm. This workshop features two semi-automatic ultrasound micro-soldering machines, with thread diameters of up to 17 µm, for ball-bonding and wedge-bonding. To verify the quality of connections, there is a micro-soldering test system for evaluating thread-resistance and solder ball shear. It also has two chip and wafer storage units for keeping ICs at optimal temperature and humidity conditions.

Chief Lab Technician

Antonio Maestre Prieto
maestre@imse-cnm.csic.es

Equipment

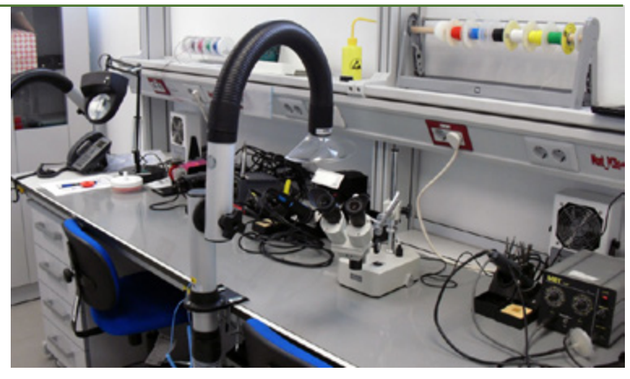
Wire Bonders, Bondtester, Ultra Low Humidity Cabinets

PCB Assembly Workshop

The PCB Assembly Workshop has all the equipment needed for soldering and desoldering thru-hole circuits mounted on PCBs, perforated matrix plates, and, in general, on any circuit-test development plates that do not require special welding techniques.

Chief Lab Technician

Antonio Maestre Prieto
maestre@imse-cnm.csic.es



Equipment

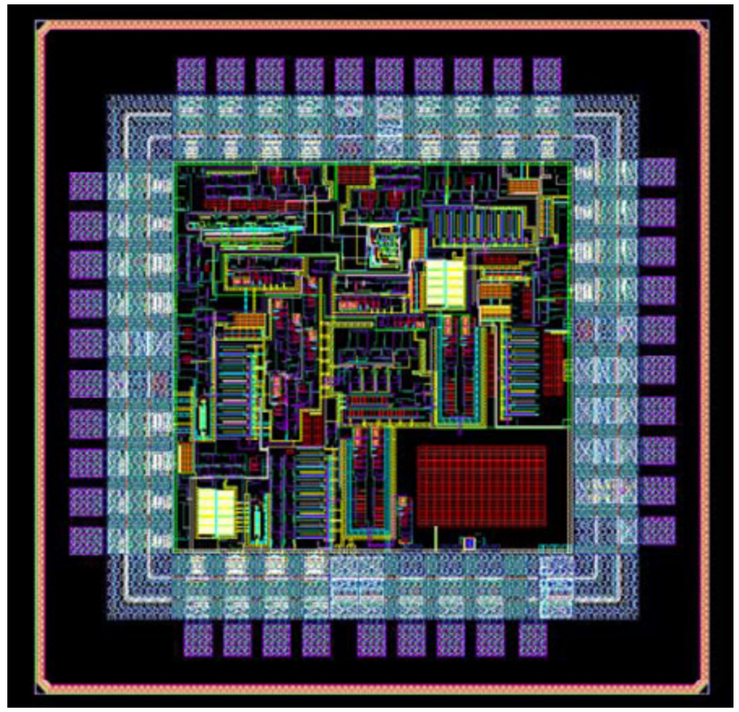
Soldering & Desoldering Stations, Ultrasonic Cleaning Bath

◆ CAD TOOLS

Most of the software tools used at the IMSE-CNM are design tools which cover several stages of the integrated circuit design process, from automatic HDL-based synthesis to the completion of full-custom layouts. As a member of the European consortium EUROPRACTICE, IMSE-CNM holds many of the licenses required by these design tools. The CAD software tool library at IMSE-CNM also includes in-house CAD tools and free-distribution tools from universities and other research centers.

CAD Manager

Dolores Vázquez Boza
lola@imse-cnm.csic.es



◆ COMMERCIAL TOOLS

Cadence Design Framework II

Analog and digital semi/full-custom design.

Cadence provides a complete integrated circuit environment allowing both analog design flows (schematic capture, electrical simulation, layout editing, design rule checking, parasitic extraction, LVS verification, etc.) and digital flows (functional description, automatic synthesis, logic simulation, automatic place & route, etc.). The environment also includes tools and languages for describing and simulating mixed analog-digital designs (AHDL, hierarchy editor, etc.).

Mentor Graphics

Analog and digital semi/full-custom design.

Mentor Graphics provides a complete integrated circuit environment allowing full digital design flow (functional description, automatic synthesis, logic simulation). This tool also covers semi-custom and full-custom layout design.

Synopsys

Simulation and VHDL synthesis.

Synopsys provides a series of HDL simulation and synthesis tools (VHDL and Verilog) for designs in both ASIC and FPGA technologies. The current distribution of this tool includes also packages for high-level synthesis, low-power synthesis, design for testability, test files and test vector generation, formal verification, temporal analysis and the use and development of IP modules.

Xilinx

FPGAs development.

Xilinx provides different tools for FPGA system design: Integrated Software Environment (ISE), a basic set of tools that facilitates the description, synthesis, implementation and verification of designs created on Xilinx CPLDs and FPGAs; Embedded Development Kit (EDK) for programmable embedded system design; ChipScope Pro, which makes it possible to

display all the signals and internal nodes of an FPGA; and System Generator for DSP, for developing digital signal processing systems on FPGAs.

Saber

Electrical simulator for mixed-signal designs.

Among other utilities, this includes: SaberHDL, a tool for simulating complex mixed-signal systems or technologies; SaberDesigner, for creating and editing designs, controlling simulations interactively and displaying and analyzing waveforms; SaberGuide, for behavioral simulation; SaberSketch, a graphical user interface; and MAST, a mixed-signal hardware description language.

Hspice

Electrical simulator.

The standard tool for simulating circuits at electrical level, this simulator makes it possible to incorporate certified device models from leading MOS device manufacturers. Featuring latest-generation simulation and analysis algorithms, it has become one of the most reliable and best known industrial circuit simulators.

Agilent Advanced Design System

Design tool for high frequency design.

The Advanced Design System (ADS) is an electronic design automation tool for RF, microwave and signal integrity applications. It uses cutting edge technologies such as 3D EM and X-parameter simulators. This tool is used by leading developers of wireless applications for communications and networks, and also by leading aerospace and defense technology companies. In one single integrated platform ADS provides design and verification standards, with wireless design libraries and EM circuit-system co-simulation, for WiMAX, LTE, multi-gigabit links and radar and satellite communications applications.

Matlab/Simulink

High-level technical computing language and interactive prototype design and development. Dynamic and embedded multi-domain simulation environment. MATLAB is a high-level technical computing language and an interactive platform for algorithm design, numerical computation and data analysis and visualization. Simulink is a tool for multi-domain simulation and design based on dynamic and embedded system models.

◆IN-HOUSE CAD TOOLS

Xfuzzy

Design of fuzzy-inference systems

Xfuzzy, the design environment for fuzzy systems, includes a set of tools that help with the design of fuzzy-logic inference-based systems, from initial description right through to final implementation. Based on the XFL specification language, Xfuzzy has tools for describing, verifying and synthesizing fuzzy systems (both software and hardware). It also features tools which allow the easy editing of package operators and hierarchical structures, tools for generating 2-D and 3-D data graphics and tools for monitoring inference processes.

Fridge

Circuit optimization using simulated annealing techniques

FRIDGE is an analog circuit optimization tool with many innovative features. It was developed to streamline the process of designing integrated circuits. FRIDGE is used to size analog circuits automatically according to design requirements. The optimization process takes place in two stages: in the first, statistical optimization techniques are applied, while deterministic techniques are applied in the second. Computational costs are drastically reduced by correctly formulating the cost function (where the designer's requirements are established) and adjusting the movement generator to match the nature of the analog sizing problem. All this can be done thanks to FRIDGE's innovative features, which include: preliminary exploration of the design space using a coarse grid to determine the best regions for further exploration, adaptive control of the temperature in the simulated annealing statistical techniques, synchronization of movement amplitude in parameter space with the temperature, etc.

Simsides

SIMulink-based SIgma-DElta Simulator

SIMSIDES is a time-domain behavioral simulator for ∑ΔMs that was developed as a toolbox in the MATLAB/SIMULINK environment. SIMSIDES can be used for simulating any arbitrary ∑ΔM architecture implemented with discrete-time (DT) or continuous-time (CT) circuit techniques.

RESEARCH AREAS & LINES

The Instituto de Microelectrónica de Sevilla is structured into Research Units whose scientific objectives focus primarily on the implementation and experimental verification of innovative concepts related to the design of micro- and nano-electronic circuits and systems.
The Research Lines developed at IMSE-CNM aim to provide solutions both in traditional sectors, such as communications, processing systems or instrumentation, and in emerging sectors, such as medical engineering, environment or space technology. These lines also consider the introduction of new devices, such as nano-sensors and micro-electro-mechanical systems (MEMS), and the use of unconventional computing paradigms, such as neural networks or fuzzy logic.

RESEARCH AREAS

- **ANALOG SIGNAL PROCESSING**
  - Analog, Mixed-Signal and Radio Frequency (AMS-RF) Circuits
  - Analog-to-Digital Converters and Mixed-Signal Interfaces
  - T est and Design-for-Test of Analog, Mixed-Signals and RF (AMS-RF) Circuits
  - Modeling, Design and Synthesis Techniques of Analog, Mixed-Signal, RF and
  - Heterogeneous Circuits and Systems
  - Low-Voltage and Low-Power Analog and Mixed-Signal Design in Deep Submicron and
  - Nanometer CMOS Technologies
  - Sigma-Delta Data Converters
- **DIGITAL SIGNAL PROCESSING & VLSI SYSTEMS**
  - CMOS Digital Intelligent and Suistainable Integrated Circuits
  - DigItal Embedded Systems and IoT
  - Cybersecurity
- **BRAIN-INSPIRED NEURAL NETWORKS AND ARTIFICIAL INTELLIGENCE**
  - Neuromorphic Cognitive Systems
  - Microelectronic Systems for Computational Intelligence
- **SENSORY & PHOTON IC VISION SYSTEMS**
  - CMOS Smart Imagers and Vision Chips
  - Heterogeneous Sensory-Processing Systems and 3-D Integration
  - Dynamic Vision Sensors
- **NANOELECTRONICS AND EMERGING TECHNOLOGIES**
  - Circuit Design using Emerging Devices and Non-Conventional Logic Concepts
  - Nanoscale Memristor Circuits and Systems
- **BIOMEDICAL AND BIOINSPIRED CIRCUITS AND SYSTEMS**
  - Biomedical Circuits and Systems
  - Wireless Implantable and Wearable Intelligent Biosensor Devices
- **INTEGRATED CIRCUITS FOR SPACE APPLICATIONS**
  - High-Speed High-Resolution ADCs & DACs for Space

RESEARCH AREA ◆ ANALOG SIGNAL PROCESSING

Analog, Mixed-Signal and Radio Frequency (AMS-RF) Circuits

Contact

Eduardo Peralías Macías
peralias@imse-cnm.csic.es

The activities of this research line focus on the development of design techniques and methodologies, mainly in advanced CMOS technologies, for analogue mixed-signal and radiofrequency circuits, with special emphasis on analogue-digital converters (ADCs) and application specific IPs (intellectual properties) for front-end analogue signal processing applications that require low power consumption, high speed and high resolution. We develop concepts such as robustness against technological variability and environmental conditions, digital calibration, self-correction and self-adjustment. All this in the framework of systems for different applications, and specifically for aerospace and wireless communications applications.

Keywords
Analog Design; Analog-to-Digital Converters; Radio Frequency Front-End; Digital Calibration; Self-Correction; Wireless and Space Applications

Research Highlights

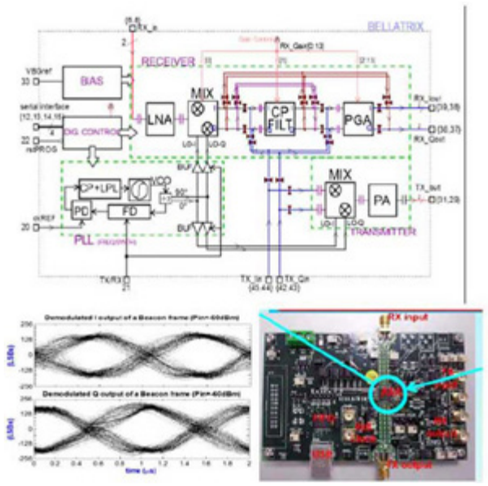
◆ J.L. Gonzalez, J.C. Cruz, R.L. Moreno and D. Vazquez, "A Proposal for Yield Improvement with Power Tradeoffs in CMOS LNAs", IEEE Latin America Transactions, vol. 14, no. 1, pp. 13-19, Jan 2016 »

◆ R. Fiorelli and E. Peralías, "Semi-empirical RF MOST model for CMOS 65nm technologies: Theory, extraction method and validation", Integration, the VLSI Journal, vol. 52, pp. 228-236, 2016 »

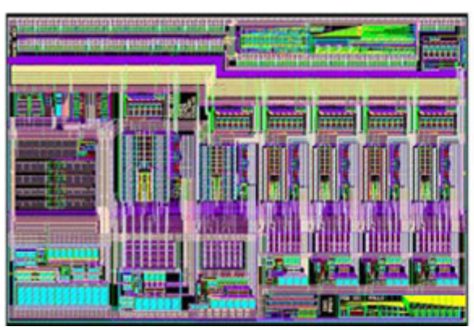
◆ A. Ginés, R. Fiorelli, A. Villegas, R. Doldán, M. Barragán, D. Vázquez, A. Rueda and E. Peralías, "Design of an Energy Efficient ZigBee Transceiver", Chap. 7 in Thomas Noulis (Ed.), Mixed-signal circuits, CRC-Press, 2015 »

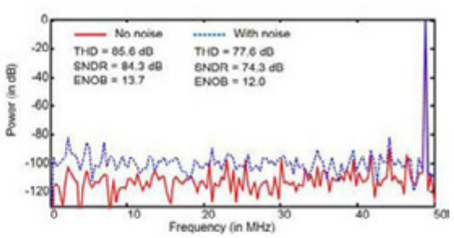
◆ A.J. Ginés, G. Leger, E. Peralías and A. Rueda, "Close-loop Simulation Method for Evaluation of Static Offset in Discrete-Time Comparators", Proceeding of the IEEE International Conference on Electronics Circuits and Systems (ICECS), Marsella, 2014 »

◆ R. Fiorelli, F. Silveira and E. Peralias, "MOST Moderate-Weak-Inversion Region as the Optimum Design Zone for CMOS 2.4-GHz CS-LNAs", IEEE Transactions on Microwave Theory and Techniques, vol. 62, no. 3, pp. 556-566, 2014 »



Caption: Prototype of a Zigbee/IEEE 802.15.4 transciever, implemented in a 1.2V 90nm CMOS technology





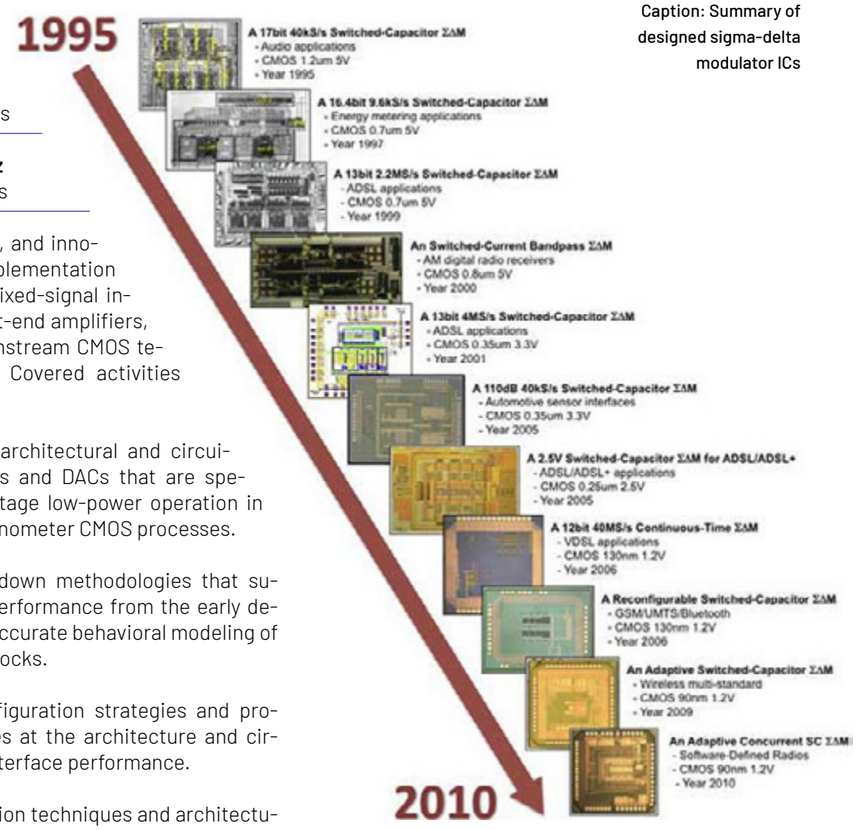
Caption: 1.8V 15-bit 100Msps Pipeline ADC: layout and post-layout simulation results of Nyquist performance with and without transient noise

Analog-to-Digital Converters and Mixed-Signal Interfaces

Contact

Ángel Rodríguez Vázquez
angel@imse-cnm.csic.es

Rocío del Río Fernández
rocio@imse-cnm.csic.es



Caption: Summary of designed sigma-delta modulator ICs

Research, development, and innovation regarding the implementation of high-performance mixed-signal interfaces, including front-end amplifiers, ADCs and DACs, in mainstream CMOS technological processes. Covered activities include:

- Exploration of novel architectural and circuital techniques for ADCs and DACs that are specially suited for low-voltage low-power operation in deep-submicron and nanometer CMOS processes.

- Development of top-down methodologies that support their optimized performance from the early design phases, including accurate behavioral modeling of mixed-signal circuital blocks.

- Exploration of reconfiguration strategies and programmability techniques at the architecture and circuit level for adaptive interface performance.

- Exploration of calibration techniques and architectures.

- Optimum chip implementation and verification.

The areas of application include wireline, wireless and optoelectronic communications, sensor interfaces, and medical electronics.

Expertise is supported by a long-term tradition (over 20 years) in the field of mixed-signal design, with special emphasis on sigma-delta, pipeline, ramp and SAR ADCs and several chips successfully transferred to industry. The accumulated know-how drives R&D, cooperation, and dissemination activities with both academia and world-leader industrial partners.

Keywords
ADCs; DACs; Mixed-Signal Interfaces; Nyquist; Sigma-Delta; Pipeline; SAR; Current-Steering; Design Methodologies; Behavioral Modeling; Performance Pptimization

Technology Transfer

Transference of a high-performance sigma-delta converter designed by our research group to Alcatel Microelectronics and STMicroelectronics for its incorporation into the ADSL2+ modem chipset ST20190 Utopia for CPE applications (massive production in 2004).

Research Highlights

◆ J. Ruiz-Amaya, M. Delgado-Restituto and A. Rodriguez-Vazquez, "Device-Level Modeling and Synthesis of High-Performance Pipeline ADCs", Springer, 2011

◆ R. del Rio, F. Medeiro, B. Perez-Verdu, J.M. de la Rosa and A. Rodriguez-Vazquez, "CMOS Cascade Sigma-Delta Modulators for Sensors and Telecom: Error Analysis and Practical Design", Springer, 2006

◆ J. Ruiz-Amaya, J.M. de la Rosa, F.V. Fernandez, F. Medeiro, R. del Rio, B. Perez-Verdu and A. Rodriguez-Vazquez, "High-Level Synthesis of Switched-Capacitor, Switched-Current and Continuous-Time ∑Δ Modulators using SIMULINK-Based Time-Domain Behavioral Mo-

dels", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 52 (9), pp. 1795-1810, 2005

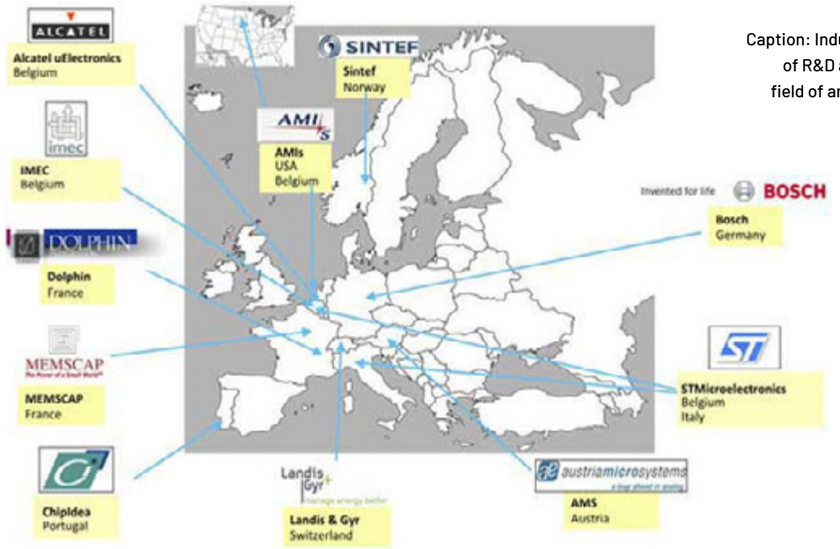
◆ A. Rodriguez-Vazquez, F. Medeiro and E. Janssens (Eds.). "CMOS Telecom Data Converters", Springer, 2003

Key Research Projects & Contracts

SPIRIT: Secured Platform for Intelligent and Reconfigurable Voice and Data Terminals (MEDEA+ 2A101)
PI: Manuel Delgado Restituto
Funding Body: MEDEA+ (European public funding)
2006 - 2009

TAMES-2: Testability of Analog Macrocells Embedded into System-on-Chip (IST 2001-34283)
PI: Belén Pérez Verdú
Funding Body: European Union (European public funding)
2002 - 2004

Design of Up-Stream and Down-Stream Data Converter for New Generation ADSL6
PI: Ángel Rodríguez Vázquez
Funding Body: Alcatel Microelectronics (European private funding) 2001 - 2003



Caption: Industrial partners of R&D activities in the field of analog-to-digital interfaces

Test and Design-for-Test of Analog, Mixed-Signals and RF (AMS-RF) Circuits

Contact

Diego Vázquez García
dgarcia@imse-cnm.csic.es

Gildas Léger
leger@imse-cnm.csic.es

Alternate Test. From a completely characterized subset of circuits, a machine-learning algorithm extracts the non-linear and multi-dimensional relations between simple signatures and specifications. This model is further used to test the rest of circuits with the simple signatures only.
This research line gathers all the activities related to the development of test techniques. These can be low-cost functional approaches whose goal is the direct estimation of the specified performance. Other structural approaches (defect-oriented or indirect) make more use of Design-for-Testability features and rely on the consideration that the circuit is correct by design. As a result, they are more focused on the detection of spot defects or unexpectedly excessive parametric deviations.
In both cases, embedded test techniques (commonly called Built-In Self-Test or BIST) are of particular interest to reduce test plan complexity, to enable the test of IP blocks with limited accessibility within a System-on-Chip (SoC) or even to enable in-field testing (which increases system-level diagnosis capability).
Our most recent research themes in this line are:

- On-line test and BIST for AMS-RF circuits.

- Characterization techniques for periodic signals and signal generation circuits for the embedded functional test of AMS circuits.

- Low-cost functional test techniques for Analog to Digital data converters.

- Machine-learning indirect test applied to AMS-RF circuits.

- Development of robust tests based on causal relationships.

Keywords
Mixed-Signal Integrated Circuits; Test; Testing; Design-for-Test (DfT); Built-In-Selft-Test (BIST); Machine-Learning

Research Highlights

◆ G. Leger and M. J. Barragan, "Brownian distance correlation-directed search: A fast feature selection technique for alternate test", Integration, the VLSI Journal, vol. 55, pp. 401–414, Sep 2016

◆ A.J. Gines E. Peralias, G. Leger, A. Rueda, G. Renaud, M.J. Barragan and S. Mir, "Linearity test of high-speed high-performance ADCs using a self-testable on-chip generator", IEEE European Test Symposium (ETS), Amsterdam, 2016

◆ M.J. Barragan and G. Leger, "A Procedure for Alternate Test Feature Design and Selection", IEEE Design & Test, vol. 32, no. 1, pp. 18–25, Feb 2015

◆ M.J. Barragan, G. Leger, D. Vazquez and A. Rueda, "On-chip sinusoidal signal generation with harmonic cancelation for analog and mixed-signal BIST applications", Analog Integrated Circuits and Signal Processing, vol. 82, pp. 67-79, 2015

◆ Best Special session award: M.J. Barragan, G. Leger, F. Azais, R.D. Blanton, A. D. Singh and S. Sunter, "Special session: Hot topics: Statistical test methods," VLSI Test Symposium (VTS), Napa (USA), 2015

Key Research Projects & Contracts

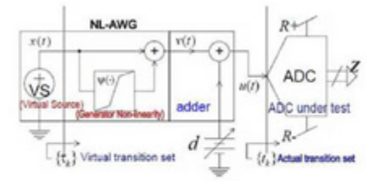
IndieTEST: Indirect Test solutions for analog, mixed-signal and RF integrated systems (PICS CNRS)
PI: Gildas Léger (CSIC) / Manuel Barragán (CNRS)
Funding Body: CSIC & CNRS
Jan 2017 - Dec 2019

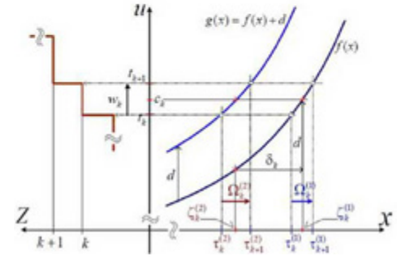
n-PATETIC: New paradigms for testing mixed-signal integrated circuits (TEC2015-68448-R)
PI: Adoración Rueda Rueda
Funding Body: Min. de Economía y Competitividad
Jan 2016 - Dec 2018

DANTE: Adapting Mixed-signal and RF ICs Design and Test to Process and Evironment Variability (TEC2011-28302)
PI: Adoración Rueda Rueda
Funding Body: Min. de Ciencia e Innovación
Jan 2012 - Dec 2014

ACATEX: Self-calibration and self-test of analog, mixed-signal and radio frecuency circuits (P09-TIC-5386)
PI: Adoración Rueda Rueda
Funding Body: Junta de Andalucía - Proyectos de Excelencia. Mar 2010 - Feb 2014

TOETS: Towards One European Test Solution
PI: José L. Huertas Díaz
Funding Body: CE: CATRENE European Program - CT302. Dec 2009 - Nov 2011





Caption: Statistical post processing for Alternate Test. From a completely characterized subset of circuits, a machine-learning algorithm extracts the non-linear and multi-dimensional relations between simple signatures and specifications. This model is further used to test the rest of circuits with the simple signatures only.

Measurement method] Caption: Measurement method for ADCs based on double-histogram. From the histograms (output code density) obtained for a non-linear monotonous input signal and its replica with an additive offset, the INL of a high-resolution ADC can be retrieved at low cost.

Modeling, Design and Synthesis Techniques of Analog, Mixed-Signal, RF and Heterog neous Circuits and Systems

Contact

Francisco V. Fernández Fernández
pacov@imse-cnm.csic.es

The general objective of this research line is to develop new modeling, design and synthesis strategies for analog, mixed-signal, radio-frequency (RF) and heterogeneous integrated circuits and systems, aiming at better performances, smaller design and fabrication cost and smaller power consumption. This also involves dealing with the increasing variability of modern technologies.
More specifically, the work includes activities in different aspects of the circuit design flow, as well as their exploitation in industrial-class designs:

- Pareto-based behavioral modeling with support to multiple hierarchical design flows.

- Layout-aware synthesis methodologies for analog/RF circuits.

- Electromagnetic-simulation-based performance modeling of passive devices for RF circuit design.

- Variability-aware design techniques.

- Development and exploitation of emerging design methodologies: bottom-up techniques, hybrid techniques and competitive strategies.

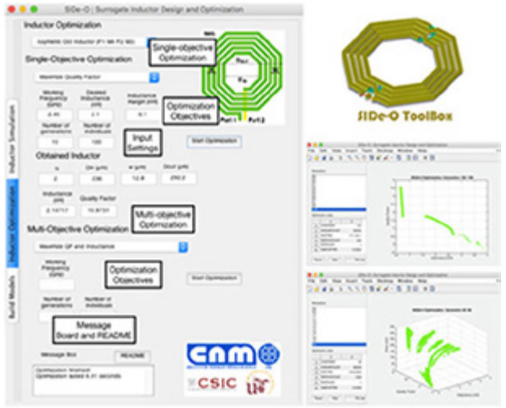
- Simulation techniques for time-zero and time-dependent variability.

Keywords
Systematic Design Methodologies; Single-Objective and Multi-Objective Optimization; Reconfigurable Design; Layout-Aware Design; Variability-Aware Design; Aging Simulation

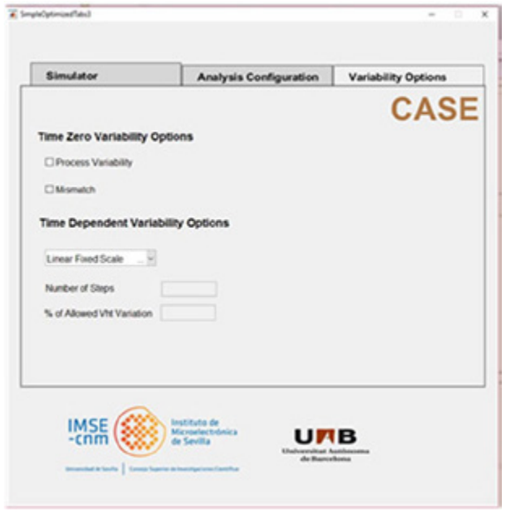
Research Highlights

◆ F. Passos, E. Roca, J. Sieiro, R. Castro-Lopez and F.V. Fernandez, "An Efficient Transformer Modeling Approach for mm-Wave Circuit Design", AEU - International Journal of Electronics and Communications, vol. 128, article 153496, 2021

◆ F. Passos, E. Roca, R. Martins, N. Lourenço, S. Ahyoune, J. Sieiro, R. Castro-Lopez, N. Horta and F. V. Fernandez, "Ready-to-Fabricate RF Circuit Synthesis using a Layout- and Variability-Aware Optimization-based Methodology", IEEE Access, vol. 8, pp. 51601-51609, 2020



Caption: Design Tool developed in the group: SIDe-O Toolbox



Caption: Design Tool developed in the group: CASE

◆ F. Passos, E. Roca, J. Sieiro, R. Fiorelli, R. Castro-Lopez, J.M. López-Villegas and F.V. Fernandez, "A multilevel bottom-up optimization methodology for the automated synthesis of RF system", IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems, vol. 39, no. 3, pp. 560-571, 2020

◆ A. Toro-Frías, P. Martín-Lloret, J. Martin-Martinez, R. Castro-López, E. Roca, R. Rodriguez, M. Nafria and F.V. Fernández, "Reliability simulation for analog ICs: Goals, solutions, and challenges", Integration - the VLSI Journal, vol. 55, pp. 341-348, 2016

◆ R. Castro-Lopez, O. Guerra, E. Roca and F.V. Fernandez, "An Integrated Layout-Synthesis Approach for Analog ICs", IEEE Trans. on Computer-Aided Design, vol. 27, no. 7, pp. 1179-1189, 2008

Key Research Projects & Contracts

VIGILANT: The Variability Challenge in Nano-CMOS - SUBPROJECT MITIGATION (PID2019-103869RB-C31)
PI: Francisco V. Fernández Fernández / Rafael Castro López
Funding Body: Min. de Ciencia, Innovación y Universidades
Jun 2020 - May 2023

TOGETHER: Towards Trusted Low-Power Things: Devices, Circuits and Architectures (TEC2016-75151-C3-3-R)
PI: Francisco V. Fernández Fernández / Rafael Castro López
Funding Body: Min. de Economía, Industria y Competitividad
Jan 2017 - Jun 2021

MARAGDA: Multilevel approach to the reliability-aware design of analog and digital integrated circuits (TEC2013-45638-C3-3-R) » web
PI: Francisco V. Fernández Fernández
Funding Body: Min. de Economía y Competitividad
2014 - 2018

KIT-LTCC: Design Kit Development in LTCC ceramic technology: modeling, simulation and fabrication of components and circuits, and design methodology (RTC-2014-2426-7)
PI: Elisenda Roca
Funding Body: Min. de Economía y Competitividad
Sep 2014 - Jan 2017

AMADEUS: Analog Modeling and Design Using a Symbolic Environment (ESPRIT IV 21821)
PI: Francisco V. Fernández Fernández
1996 - 2000

Low-Voltage and Low-Power Analog and Mixed-Signal Design in Deep Submicron and Nanometer CMOS Technologies

Contact

Óscar Guerra Vinuesa
guerra@imse-cnm.csic.es

Ángel Rodríguez Vázquez
angel@imse-cnm.csic.es

This research line embraces all activities related to the conception and design of basic building blocks and mixed-signal subsystems for system-on-chip implementation in CMOS nanometric technologies. Emphasis is placed on topologies and methods for low-voltage operation with very low power consumption. This is a transversal line whose activities intersect and provide support to the other research lines of the group. Typically building blocks and subsystems are designed for inclusion into chips implementing different system-level functions. Activities in this line include:

- Conception of new topologies for analog and mixed-signal building blocks suitable for deep submicron technologies.

- Modeling of second-order phenomena for these topologies. Embodiment of these models to support analog design flows.

- Development of design plans aimed to achieving high-performance with minimum power budget.

- Identification and exploration of fundamental limits and scaling performance of these building blocks.

- Exploration of architectural solutions for low-power operation, including power optimization, power management, smart stand-by control, etc.

- Conception of optimum architectural solutions for block programmability, error correction and calibration.

- etc.

All application areas are covered, namely, from low-noise sensor interfaces to high-frequency communications. All major analog and mixed-signal functions embedded into systems are explored. The group has been active in analog and mixed-signal design since the late eighties and through these years have devised many different kind of building blocks for smart imaging chips, automotive sensors, wireline and wireless communications, RFID, neuro-fuzzy adaptive systems, etc.

Keywords
Analog and Mixed-Signal Circuits; Synthesis, Modeling and Design; Low-Voltage; Ultra Low-Power; High-Frequency; Communications; Sensor Interfaces; Calibration

Research Highlights

◆ J.A. Rodriguez-Rodriguez, M. Delgado-Restituto, J. Masuch, A. Rodriguez-Perez, E. Alarcon and A. Rodriguez-Vazquez, "An Ultralow-Power Mixed-Signal Back End for Passive Sensor UHF RFID Transponders", IEEE Transactions on Industrial Electronics, vol. 59, no. 2, pp. 1310-1322, 2012

◆ A. Rodriguez-Perez, J. Ruiz-Amaya, M. Delgado-Restituto and A. Rodriguez-Vazquez, "A Low-Power Programmable Neural Spike Detection Channel with Embedded Calibration and Data Compression", IEEE

Transactions on Biomedical Circuits and Systems, vol. 6, no. 2, pp. 87-100, 2012

◆ J.A. Rodriguez-Rodriguez and M. Delgado-Restituto, "A low-power baseband processor for passive RFID tags employing low-power design techniques", in A.N. Laskovski (Ed.), Advances in RFID Tags, InTech, 2011

◆ J. Ruiz-Amaya, M. Delgado-Restituto and A. Rodriguez-Vazquez. "A 1.2V 10-Bit 60-MS/s 23mW CMOS Pipeline ADC with 0.67pJ/Conversion-Step and Onchip Reference Voltage Generator", Analog Integrated Circuits and Signal Processing, vol. 71, no. 3, pp. 371-381, 2011

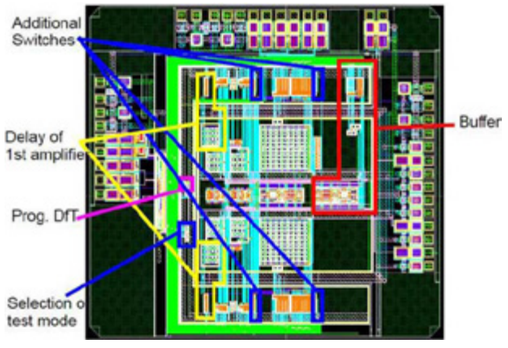
◆ J. Fernandez-Berni, R. Carmona-Galan, F. Pozas-Flores, A. Zarandy and A. Rodriguez-Vazquez. "Multi-Resolution Low-Power Gaussian Filtering by Reconfigurable Focal-Plane Binning", Proc. SPIE 8068, Bioelectronics, Biomedical, and Bioinspired Systems V; and Nanotechnology V, 806806, Prague, Czech Republic, 2011

Key Research Projects & Contracts

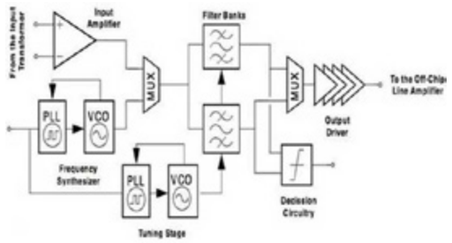
AFLS4K: Diseño micro-electrónico de un sensor lineal de alta velocidad para aplicaciones de inspección de procesos industriales (0619/0076)
PI: Óscar Guerra Vinuesa
Funding Company: Innovaciones Microelectrónicas
2009

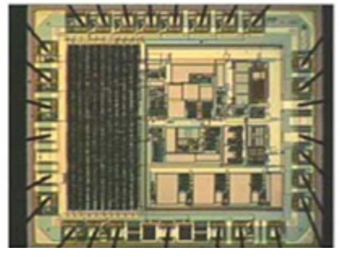
BIOTAG: Monolithic Implementation of Passive RFID Transponders for Biomedical Applications (TIC-02818)
PI: Manuel Delgado Restituto
Funding Body: Proyectos de Excelencia, Junta de Andalucía
2008

MIXMODEST: Mixed Mode In Deep Submicron Technologies (ESPRIT-29261)
PI: Ángel Rodríguez Vázquez
Funding Body: Otros Programas, Organismos Públicos Europeos
1998



Caption: Test Cirtuitry for High-Resolution ADCs





Caption: A Mixed-Signal CMOS Modem ASIC for Data Transmission on the Low-Voltage Power Line

Sigma-Delta Data Converters

Contact

José M. de la Rosa Utrera
jrosa@imse-cnm.csic.es

This research line deals with the analysis, modeling, design, implementation and experimental characterization of Sigma-Delta Modulators (SDMs) integrated in nanometer CMOS technologies. Different application scenarios are considered, spanning from sensor interfaces to broadband wireless communications. A number of Integrated Circuits (ICs) have been (and are being) developed, considering several circuit techniques, namely: discrete-time (switched-capacitor and switched-current), continuous-time (active-RC, Gm-C, Gm-LC) and hybrid continuous-time/discrete-time circuits.
The research activities carried out in the last five years have been focused on the design of SDMs intended for wireless communications, software defined radio and IoT devices. In these topics, several state-of-the-art IC prototypes have been designed in cutting-edge nanometer CMOS technologies. The design of these ICs has been supported and fueled by design methodologies and CAD tools, specifically developed to systematize the synthesis and verification procedure and to optimize the performance in terms of target specifications with minimized power consumption. An example of these CAD tools is SIMSIDES, a time-domain behavioral simulator for SDMs developed in the MATLAB/SIMULINK environment. Since the first version of SIMSIDES was developed in 2003, the tool has been continuously updated and improved with new models and facilities, and has been distributed to a number of universities, research institutes and companies all over the world.
More details can be found in www2.imse-cnm.csic.es/~jrosa

Keywords
Sigma-Delta Modulators; Analog-to-Digital Converters; Oversampling Analog-to-Digital Converters; RF-to-Digital Sigma-Delta Converters; Sigma-Delta Radio Receivers; Behavioral Modeling, Simulation and Optimization

Research Highlights

◆ J.M. de la Rosa and R. del Río, CMOS Sigma-Delta Converters: Practical Design Guide, Wiley-IEEE Press, 2018
M. Honarparvar, J.M. de la Rosa, F. Nabki and M. Sawan, "SMASH Delta-Sigma Modulator with Adderless Feedforward Loop Filter", IET Electronics Letters, vol. 8, pp. 532-534, 2017

◆ J.M. de la Rosa, R. Schreier, K.P. Pun and S. Pavan, "Next-Generation Delta-Sigma Converters: Trends and Perspectives", IEEE J. on Emerging and Selected Topics in Circuits and Systems, vol. 5, pp. 484-499, 2015

◆ G. Molina-Salgado, A. Morgado, Gordana Jovanovic-Dolecek and J.M. de la Rosa, "LC-based Bandpass Continuous-Time Sigma-Delta Modulators with Widely Tunable Notch Frequency", IEEE Trans. on Circuits and Systems - I: Regular Papers, vol. 61, pp. 1442-1455, 2014

◆ J.M. de la Rosa, "Sigma-Delta Modulators: Tutorial Overview, Design Guide and State-of-the-Art Survey", IEEE Trans. on Circuits and Systems I: Regular Papers, pp. 1-21, 2011

Key Research Projects & Contracts

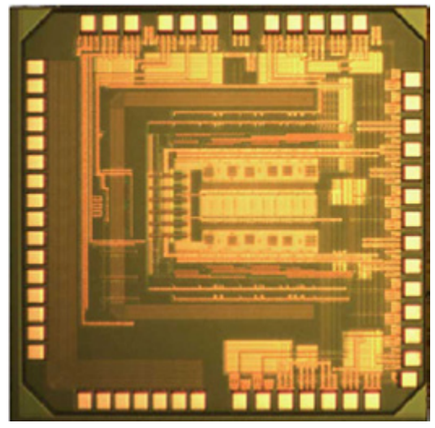
CORDION: Cognitive Radio Digitizers for IoT (PID2019-103876RB-I00)
PI: José M. de la Rosa Utrera
Funding Body: Min. de Ciencia e Innovación
Jun 2020 - Jun 2023

NEURO-RADIO: Cognitive Radio with embedded Neural Learning (US-1260118)
PI: Luis A. Camuñas Mesa / José M. de la Rosa Utrera
Funding Body: Junta de Andalucía
Jan 2020 - Jan 2022

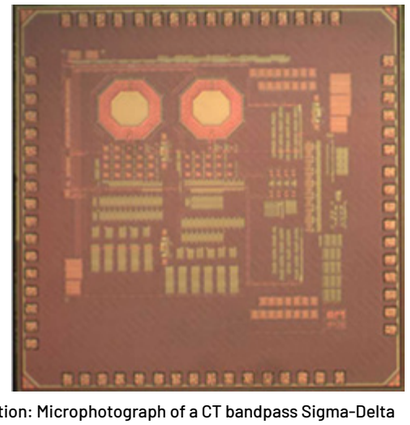
TOGHETHER: Towards Trusted Low-Power Things: Devices, Circuits and Architectures (TEC2016-75151-C3-3-R)
PI: Francisco V. Fernández Fernández & Rafael Castro López
Funding Body: Min. de Economía, Industria y Competitividad
Dec 2016 - Dec 2019

FENIX-SDR: Flexible Nanometer CMOS Analog Integrated Circuits for the Next Generation of Software-Defined-Radio Mobile Terminals (TEC2010-14825/MIC)
PI: José M. de la Rosa Utrera
Funding Body: Min. de Ciencia e Innovación
Jan 2011 - Dec 2013

ARAMIS: Adaptive RF and Mixed-signal Integrated Systems for 4G Wireless Telecom (TEC2007-67247-C02-00/MIC)
PI: José M. de la Rosa Utrera
Funding Body: C.I.C.Y.T.
Oct 2007 - Sep 2010



Caption: Microphotograph of a programmable SC lowpass cascade Sigma-Delta Modulator for SDR applications, implemented in a 90-nm CMOS technologyModulator for RF digitization, implemented using Gm-LC circuits in a 65-nm CMOS technology



Caption: Microphotograph of a CT bandpass Sigma-Delta Modulator for RF digitization, implemented using Gm-LC circuits in a 65-nm CMOS technology

RESEARCH AREA ◆ DIGITAL SIGNAL PROCESSING & VLSI SYSTEMS

CMOS Digital Intelligent and Suistainable Integrated Circuits

Contact

Antonio J. Acosta Jiménez
acojim@imse-cnm.csic.es

This research topic has as main aim the efficient implementation of digital integrated circuits on ASICs at several abstraction levels: at a transistor level, designing basic digital cells with a full-custom methodology; at a gate level, finding optimum solutions for combinational and sequential circuits; at a circuit level, developing architectures and timing strategies. Transversal optimization mechanisms are employed in all these implementations, such as for instance, switching activity analysis, minimization of power consumption, low switching-noise generation, design of cells with data-independent power consumption, design for high-speed applications, etc.
Work in this topic faces:

- Design of digital ASICS in nanometer technologies.

- Design of digital cells optimized for several parameters (i.e., dynamic power consumption, leakage, speed, area, noise, ...).

- Timing problems in digital circuits.

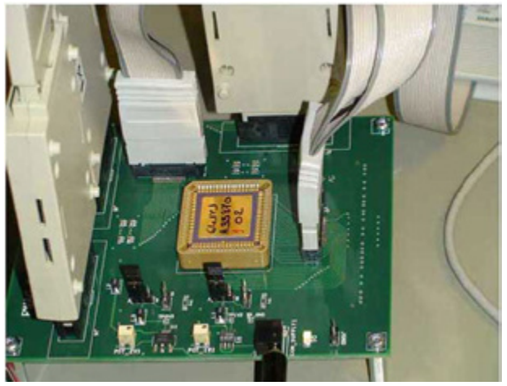
- Combined techniques for power and noise reduction in digital circuits.

Main results achieved include:
- Design, fabrication and test of digital ASICs following full-custom and semi-custom methodologies, in different technologies, including nanometric ones, for applications in control, security, communication, computational intelligence, etc.

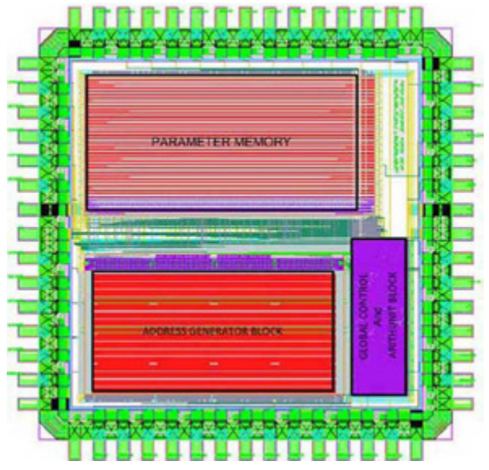
- Development of an automatic and systematic methodology for testing ASICs in the laboratory.

- Design of robust cells and circuits against timing failures, with very low power consumption, low switching-noise generation, and data-independent power consumption.

- Development of different combined noise-power (dynamic and leakage) reduction techniques.



Caption: Test board and ASIC incorporating a double-memory programmable and configurable PWAG controller



Caption: Layout of a 4-input 2-output PWA controller designed in a 90nm technology

Keywords
High-Performance Digital Design; ASICs; Timing Problems; Low-Power and Low-Noise Techniques; Design of Digital Cells

Research Highlights

◆ P. Brox, M.C. Martínez-Rodríguez, E. Tena-Sánchez, I. Baturone and A.J. Acosta, "Application specific integrated circuit solution for multi-input multi-output piecewise-affine functions", International Journal of Circuit Theory and Applications, vol. 44, no. 1, pp. 4-20, 2016

◆ M.C. Martínez-Rodríguez, P. Brox and I. Baturone, "Digital VLSI implementation of piecewise-affine controllers based on lattice approach", IEEE Transactions on Control Systems Technology, vol. 23, no. 3, pp. 842-854, 2015

◆ A.J. Acosta, "Low Power and Security Trade-off in Hardware: From True Random Number Generators to DPA Resilience", Conferencia invitada al Energy Secure Systems Architecture Workshop ISCA 2014, Minnessotta, USA

◆ P. Brox, J. Castro-Ramírez, M.C. Martínez-Rodríguez, E. Tena, C.J. Jiménez, I. Baturone and A.J. Acosta, "A Programmable and Configurable ASIC to Generate Piece-wise-Affine Functions Defined Over General Partitions", IEEE Trans. on Circuits and Systems I: Regular Papers, vol. 60, no. 12, pp. 3182-3194 , 2013
Technology Transfer

◆ A.J. Acosta, I. Baturone, J. Castro-Ramírez, C.J. Jiménez, P. Brox and M.C. Martínez-Rodríguez. Method for generating piecewise-affine multivariable functions with on-line computation of the search tree and device for implementing same. 2012

Key Research Projects & Contracts

INTERVALO: Integration and validation in laboratory of countermeasures against side-channel attacks in microelectronic cryptocircuits (TEC2016-80549-R)
PI: Antonio J. Acosta Jiménez / Carlos J. Jiménez Fernández
Funding Body: Min. de Economía, Industria y Competitividad
Dec 2016 - Dec 2019

CESAR: Secure microelectronic circuits against side-channel attacks (TEC2013-45534-R) » web
PI: Antonio J. Acosta Jiménez / Carlos J. Jiménez Fernández
Funding Body: Min. de Economía y Competitividad
Jan 2014 - Dec 2016

CITIES: Integrated circuits for transmitting secure information (TEC2010-16870) » web
PI: Carlos J. Jiménez Fernández
Funding Body: Min. de Ciencia e Innovación
Jan 2011 - Sep 2014

MOBY-DIC: Model-based synthesis of digital electronic circuits for embedded control (EC-IST-VIIPM no.-248858)
PI: Antonio J. Acosta Jiménez
Funding Body: 7th Framework Programme, European Commission
Dec 2009 - Nov 2013

CRIPTO-BIO: Microelectronic design for crypto-biometric authentication (P08-TIC-03674) » web
PI: Iluminada Baturone Castillo
Funding Body: Junta de Andalucía - Proyectos de Excelencia
Jan 2009 - Dec 2013

Digital Embedded Systems and IoT

Contact

Ángel Barriga Barros
barriga@imse-cnm.csic.es

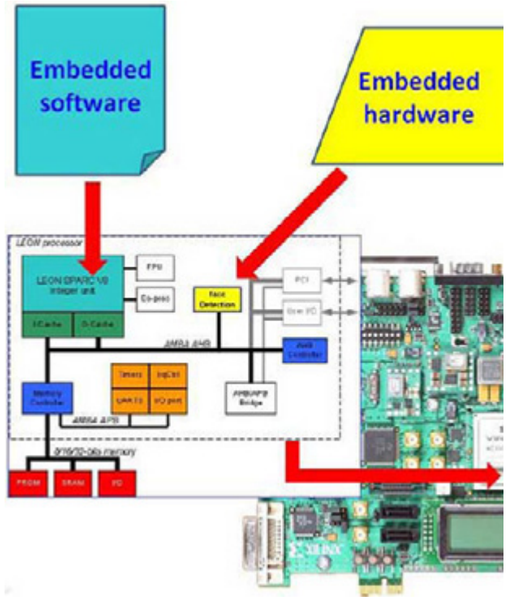
This research line is focused on the design of digital embedded systems implemented on programmable devices (FPGAs), using intellectual property (IP) modules. The aim is to solve problems related to size constraints, power consumption and computation that characterize such systems, as well as to provide the tools and design methodologies that facilitate and accelerate its development. The highlights of the developed solutions are the design of specific processing architectures, hardware/software codesign techniques, the use of reconfigurable devices, and the employment of Intellectual Property (IP) modules for reusability. The transversal nature of this research line allows that its results can be used in different application domains related to other research activities of the group.
The topics of interest that are covered by this research line are:

- Development of design methodologies for embedded digital systems.
  · Specification languages.
  · Hardware & software codesign.
  · CAD tools development.

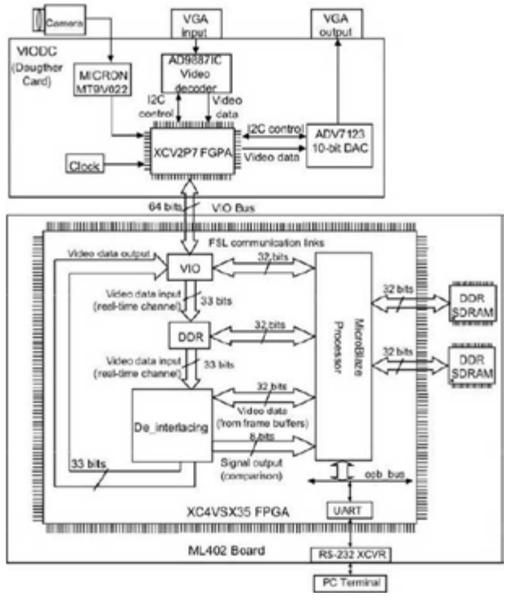
- Architectures for specific application systems.
  · Architectures and design of data/signal processing modules
  · Development of IP modules.
  · Reconfigurable systems

- Applications of embedded digital systems.
  · Biometric systems based on fingerprint, face and voice.
  · Cryptographic systems
  · Image processing and artificial vision
  · Emerging applications of wearables, smart cards, communications networks, industrial control systems, wireless sensor networks and Internet of Things.

Keywords
Embedded Systems; Design Methodologies; Systems



Caption: FPGA-Based Embedded System to Implement Viola-Jones Face Detection Algorithm



Caption: FPGA-Based Embedded System for Video De-Interlacing. a) Block Diagram. b) Experimental Setup

on Chip (SoC); Hardware & Software Codesign; Reconfigurable Devices; CAD Tools

Research Highlights

◆ M.J. Avedillo, A. Barriga, L. Acasandrei and J.M. Calahorro, "Hardware-software embedded face recognition system", International Conferences in Central Europe on Computer Graphics, Visualization and Computer Vision (WSCG), Pilzen, Czech Republic, 2016

◆ E. Calvo-Gallego, P. Brox and S. Sanchez-Solano, "Low-cost dedicated hardware IP modules for background subtraction in embedded vision systems", Journal of Real-Time Image Processing, vol. 12, no. 4, pp. 681-695, 2016

◆ P. Brox, I. Baturone and S. Sánchez-Solano, "Fuzzy logic-based embedded system for video de-interlacing", Applied Soft Computing, vol. 14, part C, pp. 338-346, 2014

◆ M. Brox, S. Sánchez-Solano, E. del Toro, P. Brox and F.J. Moreno-Velo, "CAD tools for hardware implementation of embedded fuzzy systems on FPGAs", IEEE Transactions on Industrial Informatics, Special Section on Embedded and Reconfigurable Systems, vol. 9, no. 3, pp. 1635-1644, 2013

Key Research Projects & Contracts

ID-EO: Design of crypto-biometric hardware for video encryption and authentication (TEC2014-57971-R)
PI: Iluminada Baturone Castillo / Piedad Brox Jiménez
Funding Body: Min. de Economía y Competitividad
Jan 2015 - Dec 2018

SENIAC: Security in interconnected devices by injection of authentication and ciphering algorithms (RTC-2014-2932-8)
PI: Iluminada Baturone Castillo
Funding Body: Min. de Economía y Competitividad
Oct 2014 - Mar 2017

SEIs: Hardware design for embedded systems in intelligent environments (TEC2011-24319)
PI: Santiago Sánchez Solano
Funding Body: Min. de Ciencia e Innovación
Jan 2012 - Sep 2015

MOBY-DIC: Model-based synthesis of digital electronic circuits for embedded control (EC-IST-VIIPM no.-248858)
PI: Antonio J. Acosta Jiménez
Funding Body: 7th Framework Programme, European Commission
Dec 2009 - Nov 2013

CRIPTO-BIO: Microelectronic design for crypto-biometric authentication (P08-TIC-03674)
PI: Iluminada Baturone Castillo
Funding Body: Junta de Andalucía - Proyectos de Excelencia
Jan 2009 - Dec 2013

RESEARCH AREA ◆ BRAIN-INSPIRED NEURAL NETWORKS AND ARTIFICIAL INTELLIGENCE

Neuromorphic Cognitive Systems

Contact

Bernabé Linares Barranco
bernabe@imse-cnm.csic.es

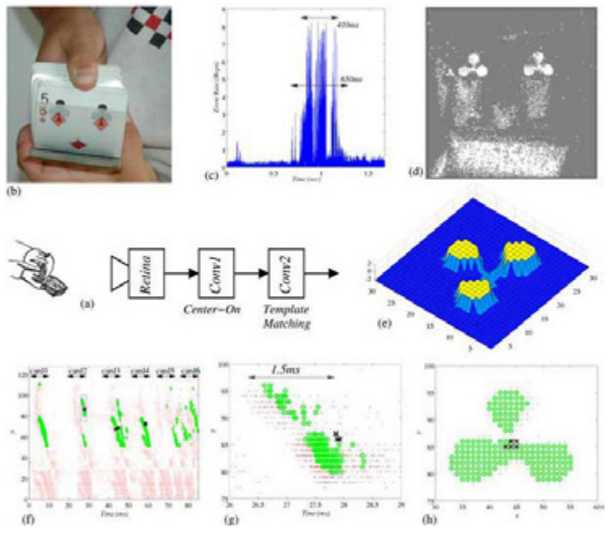
Teresa Serrano Gotarredona
terese@imse-cnm.csic.es >

Luis A. Camuñas Mesa
camunas@imse-cnm.csic.es >

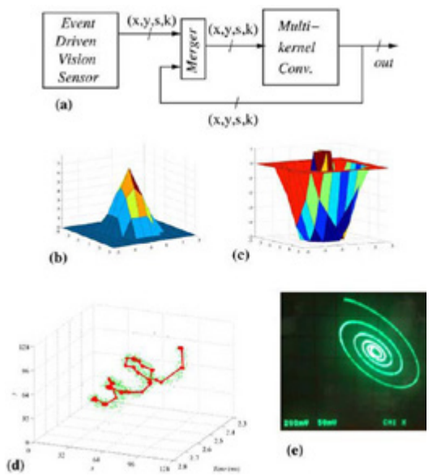
The IMSE Neuromorphic group develops sensory and processing microchips that mimic sensing and processing in biological beings. It also develops multi-chip and hybrid chip-FPGA systems to scale up to higher complexity systems. The group also works on algorithms and sensory processing for spiking information sensing, coding and processing. Chips use mixed signal, low current, and/or low power, circuit techniques, as well as high speed communication techniques. The group uses mixed or digital CMOS technologies, as well as application projections exploiting emergent nanoscale technologies or new devices like memristors.
At present, the group focuses mainly on event-driven (spiking) frame-free vision systems, developing sensing retinas for spatial or temporal contrast (such as DVS -Dynamic Vision Sensors), as well as event-driven convolution processors, which allow to assemble for example large scale spiking 'Convolutional Neural Networks' for high speed object recognition. These chips and systems use AER (Address Event Representation) communication techniques.
Event-driven retinas do not produce sequences of still frames, as conventional video cameras do. Instead, each pixel senses light and computes a given property (spatial contrast, temporal change) continuously in time. Whenever this property exceeds a given threshold, the pixel sends out an event (which usually consists of the pixel x,y coordinate and the sign of the threshold), which is written onto one (or more) high speed bus with asynchronous handshaking. This way, sensors produce continuous event flows, and subsequent processors process them event by event.

Keywords

Spiking Neural-Circuits; Signal-Processing; Learning; AER (Address-Event-Representation); AER-Contrast-Retinas; AER Dynamic Vision Sensors (DVS); Memristive Neuromorphic Systems; AER-Processors; AER-Convolution; STDP (Spike-Timing-Depen-



Caption: Event-driven shape sensing-recognition. (a) system, (b) stimulus, (c) events, (d-f) stages outputs showing 'clover' recognition simultaneous to stimulus. See ref [B] for details.



Caption: Event-driven sensing-processing system with (a) DVS-retina and multi-kernel-convolver (b,c): it captures the 500Hz oscilloscope spiral (e), generating events (x,y,t), representing the spatio-temporal trajectory (d). See ref [A] for details.

dent-Plasticity); Low-Power; Frame-Free-Vision; Convolutional-Neural-Networks

Research Highlights

◆ A. Yousefzadeh, M. Khoei, S. Hosseini, P. Holanda, S. Leroux, O. Moreira, J. Thapson, B. Dhoet, P. Simoens, T. Serrano-Gotarredona, and B. Linares-Barranco, "Asynchronous Spiking Neurons, the natural key to exploit temporal sparsity", IEEE Journal on Emergent and Selected Topics in Circuits and Systems, vol. 9, no. 4, pp. 668-678, 2019

◆ A. Yousefzadeh, E. Stromatias, M. Soto, T. Serrano-Gotarredona and B. Linares-Barranco, "On Practical Issues for Stochastic STDP Hardware with 1-bit Synaptic Weights", Frontiers in Neuroscience, vol. 12, article 665, 2018

◆ A. Yousefzadeh, M. Jablonski, T. Iakymchuk, A. Linares-Barranco, A. Rosado, L.A. Plana, S. Temple, T. Serrano-Gotarredona, S. Furber, and B. Linares-Barranco, "On Multiple AER Handshaking channels over High-Speed Bit-Serial Bi-Directional LVDS Links with Flow-Control and Clock-Correction on Commercial FPGAs for Scalable Neurmorphic Systems", IEEE Trans. on Biomedical Circuits and Systems, vol 11, no. 5, pp. 1133-1147, 2017

◆ [B] J. A. Pérez-Carrasco, B. Zhao, C. Serrano, B. Acha, T. Serrano-Gotarredona, S. Chen and B. Linares-Barranco, "Mapping from Frame-Driven to Frame-Free Event-Driven Vision Systems by Low-Rate Rate-Coding and Coincidence Processing. Application to Feed-Forward ConvNets," IEEE Trans. on Pattern Analysis and Machine Intelligence, vol. 35, no. 11, pp. 2706-2719, 2013

◆ [A] L. Camuñas-Mesa, C. Zamarreño-Ramos, A. Linares-Barranco, A. Acosta-Jiménez, T. Serrano-Gotarredona and B. Linares-Barranco, "An Event-Driven Multi-Kernel Convolution Processor Module for Event-Driven Vision Sensors," IEEE Journal of Solid-State Circuits, vol. 47, no. 2, pp. 504-517, 2012

Technology Transfer
Spin-off Company: Prophesee. Metavision for machines
Spin-off Company: GrAI Matter Labs. Create magic on the edge with GrAI One

Key Research Projects & Contracts

SPINAGE: Weighted Spintronic-Nano-Oscillator-based Neuromorphic Computing System Assisted by laser for Cognitive Computing
PI: Teresa Serrano-Gotarredona
Funding Body: European Union
Oct 2020 - Sep 2024

NeurONN: Two-Dimensional Oscillatory Neural Networks for Energy Efficient Neuromorphic Computing
PI: Bernabé Linares-Barranco
Funding Body: European Union
Jan 2020 - Dec 2022
HBP: Human Brain Project
PI: Bernabé Linares-Barranco
Funding Body: European Union
Apr 2014 - Mar 2016

NABAB: Nanocomputing Building Blocks with Acquired Behaviour
PI: Teresa Serrano Gotarredona
Funding Body: European Union
Apr 2007 - Apr 2010

CAVIAR: Convolution AER Vision Architecture
PI: Bernabé Linares-Barranco
Funding Body: European Union
Jun 2002 - Jun 2006s

Microelectronic Systems for Computational Intelligence

Contact

Santiago Sánchez Solano
santiago@imse-cnm.csic.es

This research line focuses on the development of new design methodologies and circuit elements for Computational Intelligence applications. Computational Intelligence includes a set of techniques inspired by natural processes that allow addressing complex problems more efficiently than through traditional approaches. Specifically, our interest is mainly focused towards efficient hardware implementation of neuro-fuzzy systems and its use in applications that take advantage of their ability to describe a system with linguistic terms, as well as to cope with the inaccurate, vague or incomplete information that appears in many real-world problems.
In recent years, the developed activities in this line have addressed the following three main objectives:
- The development of architectures for efficient implementation of fuzzy-inference systems on ASICs and FPGAs, as well as the proposal of a model-based design methodology that accelerates the stages of functional verification and synthesis of fuzzy modules and facilitates their integration in embedded systems.

- The generation of a development environment for fuzzy systems, Xfuzzy, which facilitates the tasks of design, verification and synthesis, both software and hardware, of fuzzy logic-based systems.
- The application of the above techniques and circuits to different problems of robotics, industrial control, food technology, communications systems, image processing, and intelligent device networks for applications related to the areas of safety and environmental control.

Keywords
Intelligent Systems; Soft-Computing; Neuro-Fuzzy Circuits; CAD Tools; Model-Based Design; Fuzzy Control; Fuzzy Image Processing; Internet of Things

Research Highlights

◆ S. Sánchez-Solano and M. Brox, "Hardware Implementation of Embedded Fuzzy Controllers on FPGAs and ASICs", in Fuzzy Modelling and Control: Theory and Applications, vol. 9, pp. 235-253, Atlantis Series on Computational Intelligence Systems, Springer-Verlag, 2014

◆ S. Sánchez-Solano, E. del Toro, M. Brox, P. Brox and I. Baturone, "Model-Based Design Methodology for Rapid Development of Fuzzy Controllers on FPGAs", IEEE Trans. on Industrial Informatics, vol. 9, no. 3, pp. 1361-1370, 2013

◆ P. Brox, I. Baturone and S. Sánchez-Solano, "Fuzzy Logic-Based Algorithms for Video De-Interlacing", Series: Studies in Fuzziness and Soft Computing, vol. 246, Springer, 2010

◆ S. Sánchez-Solano, A. J. Cabrera, I. Baturone, F.J. Moreno-Velo and M. Brox, "FPGA Implementation of Embedded Fuzzy Controllers for Robotic Applications", IEEE Trans. on Industrial Electronics, vol. 54, no. 4, pp. 1937-1945, 2007

◆ I. Baturone, A. Barriga, S. Sánchez-Solano, C.J. Jiménez-Fernández and D.R. López, Microelectronic Design of Fuzzy Logic-Based Systems, CRC Press, 2000

Key Research Projects & Contracts

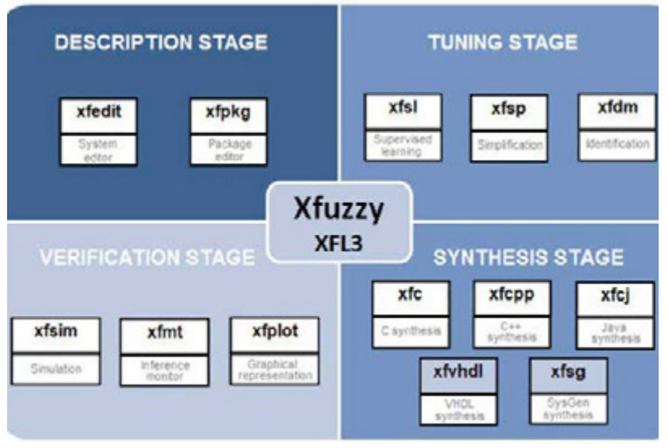
Predicción regional de potencia eólica a partir de Lógica Difusa
PI: Iluminada Baturone Castillo
Funding Body: EDP Renováveis
2014 - 2015

SEIs: Diseño hardware para sistemas empotrados en entornos inteligentes (TEC2011-24319)
PI: Santiago Sánchez Solano
Funding Body: Min. de Ciencia e Innovación
Jan 2012 - Sep 2015

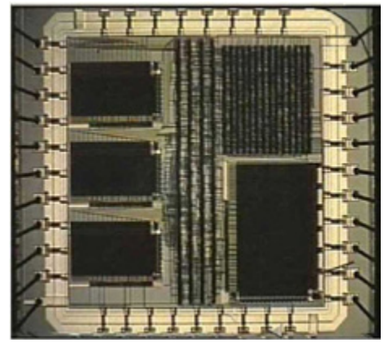
DIMISION: Diseño microelectrónico de sistemas de visión para redes de sensores inteligentes (TEC2008-04920)
PI: Santiago Sánchez Solano
Funding Body: Min. de Ciencia e Innovación
Jan 2009 - Jun 2012

FVISION: Implementación microelectrónica de circuitos difusos para microsistemas inteligentes de visión (TEC2005-04359/MIC)
PI: Ángel Barriga Barros
Funding Body: Min. de Ciencia y Educación
Dec 2005 - Dec 2008

Diseño microelectrónico de sistemas inteligentes para el procesado de información sensorial (TIC2001-1726-C02-01)
PI: Santiago Sánchez Solano
Funding Body: Gobierno de España
2001-2004



Caption: VLSI implementation of a 3-input 1-output fuzzy inference system using an active rule-based architecture.



Caption: Components of the Xfuzzy environment, which integrates tools to facilitate the different stages involved in the design process of fuzzy logic-based systems.

RESEARCH AREA ◆ SENSORY & PHOTONIC VISION SYSTEMS

CMOS Smart Imagers and Vision Chips

Contact

Ángel Rodríguez Vázquez
angel@imse-cnm.csic.es

Ricardo Carmona Galán
rcarmona@imse-cnm.csic.es

Image handling is instrumental in many applications, including consumer electronics, surveillance, robotics, machine vision, etc. Some of them demand high quality images, while others require fast analysis and interpretation of the image flow. Despite the specific target, all applications benefit from embedding processing circuitry together with optical sensors in the same silicon substrate. CMOS technologies allow the incorporation of digital processing on-chip to correct image artifacts or to analyze and interpret the scene in real-time. Using CMOS technologies enables the implementation of cameras and vision systems with reduced power consumption and reduced size. This permits the incorporation of vision in applications where it was previously considered to be economically prohibitive or technically unfeasible.
This research line embraces different activities related to the incorporation of intelligence into image sensors, namely:
- New pixel topologies for enhanced sensitivity and reduced noise.

- Front-side and Back-side illuminated sensors.

- Pixels for single-photon detection and time-of-flight calculations.

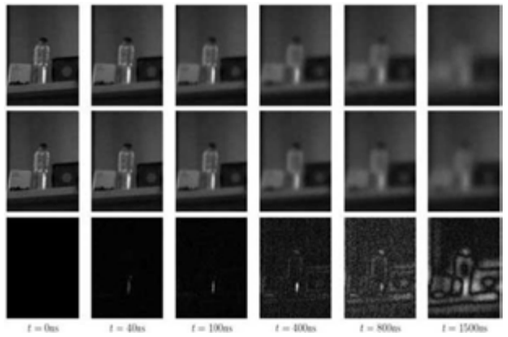
- Pixels for high-dynamic range image acquisition.

- In-pixel processing and memory for feature extraction at the focal-plane.

- Re-configurable read-out channels for high-performance digital imagers.

- Data converters for high-speed and high accuracy (low noise) image downloading.

- Architectures and algorithms for on-chip image correction.



Caption: On-chip generated scale-space (upper row) compared to ideal (middle row). Gaussian filters are implemented by time-controlled diffusion.

- Distributed, progressive processing architectures for vision systems.

- Sensors for 3-D image capture.

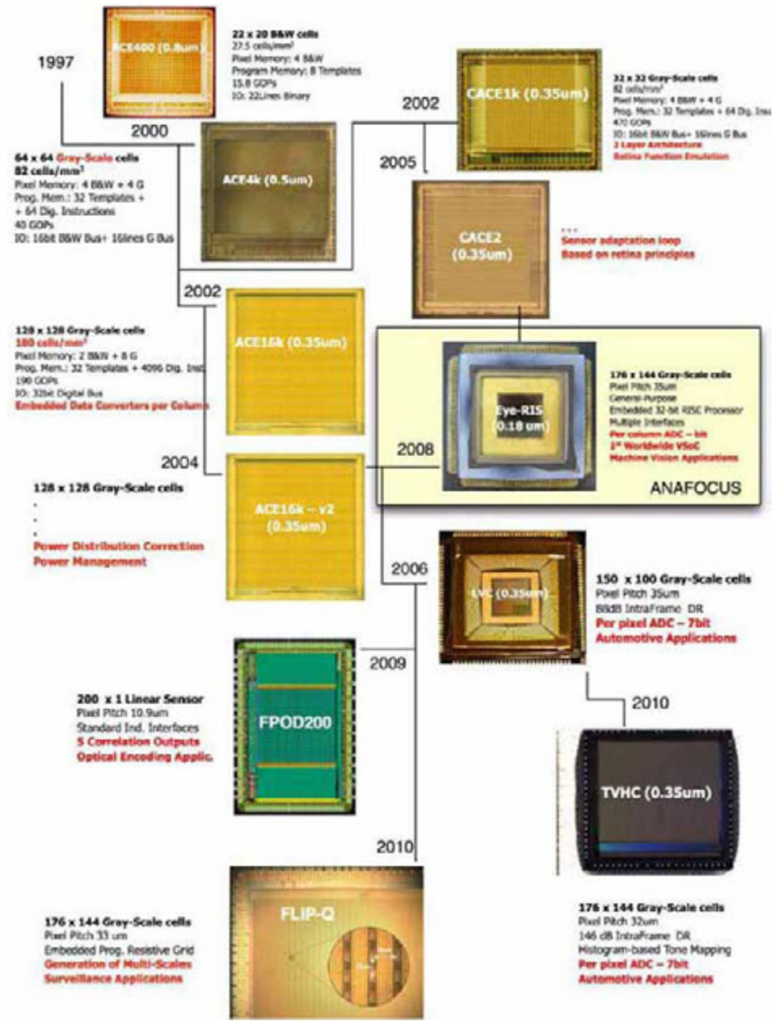
Different application areas are covered like automotive, unmanned vehicle navigation, distributed smart cameras and vision-enabled wireless sensor networks. These applications have been benchmarked by using real systems. Significant parts of the technology have been transferred to industry, including the creation of spin-off companies.

Keywords
Smart CMOS Imagers; HDR Imagers; Real-Time Vision Systems-on-Chip; Data Converters for Imagers; Silicon Retinas

Research Highlights

◆ J. Fernandez-Berni, R. Carmona-Galan and A. Rodriguez-Vazquez, Low-Power Smart Imagers for Vision-Enabled Sensor Networks, Springer, 2012

◆ J. Fernandez-Berni, R. Carmona-Galan and L. Carranza-Gonzalez. "FLIP-Q: A QCIF Resolution Focal-Plane Array for Low-Power Image Processing", IEEE Journal of Solid-State Circuits, vol. 46, no. 3, pp. 669-680, 2011
G. Liñan, A. Rodriguez-Vazquez, R. Carmona, F. Jimenez, S. Espejo and R. Dominguez-Castro, "A 1000 FPS@128x128 Vision Processor with 8-bit Digitized I/O", IEEE Journal of Solid-State Circuits, vol 39, no. 7, pp. 1044-1055, 2004



Chronology of the vision chips designed by the group, from 1997 to 2010

◆ A. Rodriguez-Vazquez, G. Liñan, L. Carranza, E. Roca, R. Carmona, F. Jimenez-Garrido, and R. Dominguez-Castro, "ACE16k: the Third Generation of Mixed-Signal SIMD-CNN ACE Chips towards VSoCs", IEEE Transactions on Circuit and Systems I: Fundamental Theory and Applications, vol. 51, no. 5, pp. 851-863, 2004

◆ T. Roska and A. Rodriguez-Vazquez (Eds.), Towards the Visual Microprocessor: VLSI Design and the Use of Cellular Neural Network Universal Machine Computers, pp. 213-237, John Wiley & Sons, 2001

Key Research Projects & Contracts

3DHVC: Design of high-performance heterogeneous, ultra high speed cellular sensor-processors for multispectral light sensing (BAA-11-001)
PI: Ángel Rodríguez Vázquez
Funding Body: Office of Naval Research (USA)
Jan 2011 - Dec 2013

WIVISNET: Wireless and smart vision sensors for networked surveillance and monitoring (TEC2009-11812)
PI: Ricardo Carmona Galán
Funding Body: Min. de Ciencia e Innovación
Jan 2010 - Dec 2012

VISTA: Design of sensing-processing-actuation systems on-a-chip: 4th generation vision systems (TIC2003-09817-C02-C01)
PI: Ángel Rodríguez Vázquez
Funding Body: Min. de Ciencia y Tecnología
Dec 2003 - Nov 2006

Heterogeneous Sensory-Processing Systems and 3-D Integration

Contact

Ángel Rodríguez Vázquez
angel@imse-cnm.csic.es

Ricardo Carmona Galán
rcarmona@imse-cnm.csic.es

3D Integration technologies enable vertical interconnection of different wafers and thus the allocation of different subsystems and functions into dedicated, specialized layers. Both features have significant impact on performance. On the one hand, different technologies and materials can be combined, for instance nano-antennas for THz radiation detectors. On the other hand, form factors can be improved and larger function densities can be achieved; for instance, image pixels with embedded processing can be effectively implemented without penalizing the fill factor and the pixel pitch.
This research comprises different activities concerning heterogeneous sensory-processing systems using 3D IC with emphasis on technologies employing TSVs.
Activities include the following:
- Prospective analysis and identification of suitable 3D technology candidates.

- Multi-spectral, 3D-compatible sensing materials and devices.

- Interface circuitry between these sensors and the processing layers, including the electrical interface itself as well as the time multiplexing which may be required to handle different signal granularities at the different layers.

- Architectures for optimum exploitation of the potentials of 3D heterogeneous technologies. Emphasis is on vision systems and the usage of different spatial resolutions and scales at each layer in the vertically-interconnected architecture.

- Identification of constitutive functional operators for the different layers of the vertical processing chain, with emphasis on vision.

- Circuit topologies for the different layers of the processing chain.

Regarding vision systems, the basic challenge is to achieve sensors with million pixel counts, pixel pitch around 6μm and operating speed in the range of 10,000 Frames/second.

Keywords
3D Integrated Circuits; Through-Silicon-Vias; Vertically-Interconnected Systems; Heterogeneous Integration

Research Highlights

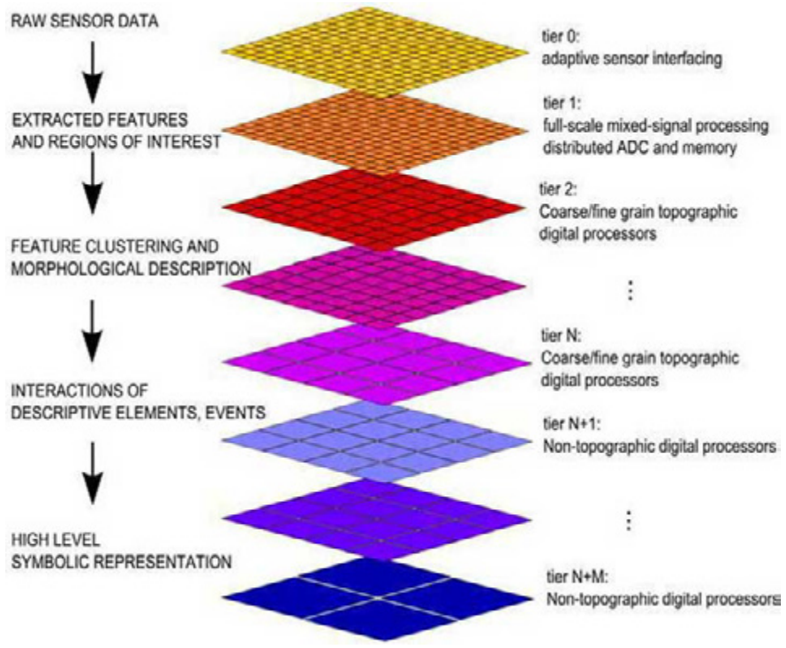
◆ R. Carmona-Galan, A. Zarandy, Cs. Rekeczky, P. Földesy, A. Rodriguez-Perez, C. Dominguez-Matas, J. Fernandez-Berni, G. Liñan-Cembrano, B. Perez-Verdu, Z. Karasz, M. Suarez-Cambre, V. M. Brea-Sanchez, T. Roska and A. Rodriguez-Vazquez, "A hierarchical vision processing architecture oriented to 3D integration of smart camera chips", Journal of Systems Architecture, vol. 69, no. 10, part A, pp. 908-919, 2013

◆ M. Suarez, V.M. Brea, J. Fernandez-Berni, R. Carmona-Galan, G. Liñan, D. Cabello and A. Rodriguez-Vazquez, "CMOS-3D Smart Imager Architectures for Feature Detection", IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 2, no. 4, pp. 723-736, 2012

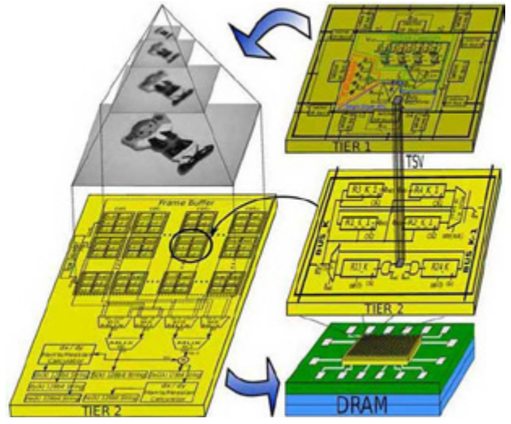
◆ A. Zarandy, Cs. Rekeczky, P. Földesy, R. Carmona-Galan, G. Liñan-Cembrano, G. Sos, A. Rodriguez-Vazquez and T. Roska, "VISCUBE: a multi-layer vision chip", in Á. Zarandy (Ed.), Focal-Plane Sensor-Processor Chips, pp. 181-208, Springer, 2011

◆ A. Zarandy, P. Földesy, R. Carmona-Galan, Cs. Rekeczky, J. Bean and W. Porod, "Cellular Multi-core Processor Carrier Chip for Nanoantenna Integration and Experiments", in Ch. Baatar, W. Porod & T. Roska (Eds.), Cellular Nanoscale Sensory Wave Computing, , pp. 147-168, Springer, 2010

◆ R. Maldonado-Lopez, F. Vidal-Verdu, G. Liñan and A. Rodriguez-Vazquez, "Integrated Circuitry to Detect Slippage Inspired by Human Skin and Artificial Retinas", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 56, no. 8, pp. 1554-1565, 2009



Caption: Functional/ physical mapping in a multilayer structure



Caption: A CMOS-3D reconfigurable architecture with In-pixel processing for feature detectors

Key Research Projects & Contracts

INNPACTO 3D2: Intelligent Image Sensors in CMOS Technology with 3D Stacked Chips (IPT-2011-1625-430000)
PI: Ángel Rodríguez Vázquez
Funding Body: Min. de Ciencia e Innovación
May 2011 - Dec 2014

3DHVC: Design of high-performance heterogeneous, ultra high speed cellular sensor-processors for multispectral light sensing (BAA-11-001)
PI: Ángel Rodríguez Vázquez
Funding Body: Office of Naval Research, USA
Jan 2011 - Dec 2013

Study and design of interfaces for CMOS-compatible sensing nanostructures for the integration of nanoelectronic systems
PI: Ricardo Carmona Galán
Funding Body: Min. de Educación y Ciencia
Oct 2006 - Sep 2007

Dynamic Vision Sensors

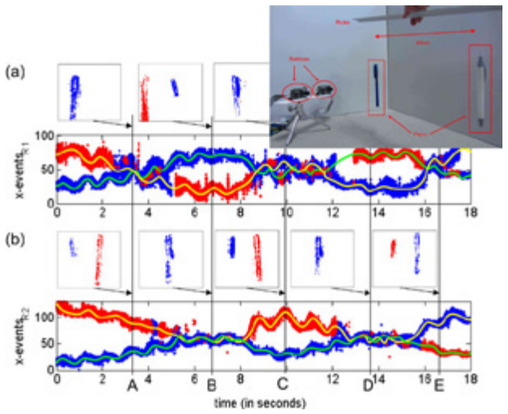
Contact

Bernabé Linares Barranco
bernabe@imse-cnm.csic.es

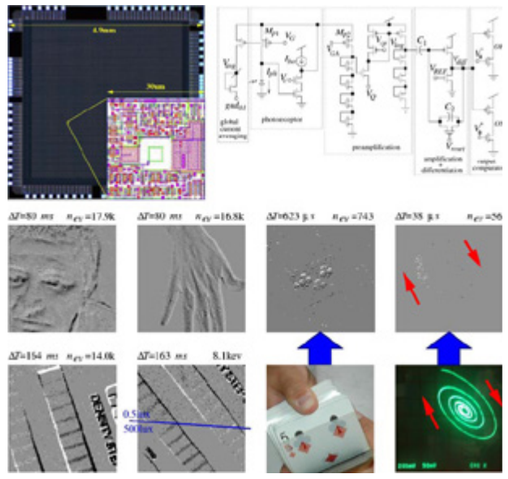
Teresa Serrano Gotarredona
terese@imse-cnm.csic.es

Luis A. Camuñas Mesa
camunas@imse-cnm.csic.es

Dynamic Vision Sensors are a type of spiking silicon retinas in which each pixel autonomously and asynchronously sends out an address event when the light it senses has changed above a given relative threshold. This type of cameras, which are "Frame-Free", do not generate sequences of still frames, as conventional commercial cameras do, but provide a flow of spiking address events that dynamically represent the changing visual scene. They are heavily inspired in biological retinas, which also send continuously nervous spike impulses to the cortex. Biological retinas are continuously vibrating through microsaccades and ocular tremors, thus producing spikes also when there is change of light. DVS cameras provide an almost instantaneous representation (with micro-second delays) of the changing visual reality, with very reduced data flow, reduced power, and data sparsity, thus reducing data processing requirements of subsequent stages. DVS cameras have become of high interest to industry recently with a number of spinoff companies commercializing them (Prophesee, IniVation, Celepixel as well as large traditional companies like Samsung and Sony embracing developments.
At IMSE there is a specific research line on AER (Address Event Representation) DVS cameras by the Neuromor-



Caption: 3D Stereo Vision with a pair of DVS cameras solving correct object tracking with temporal occlusions. See ref [B] for details.



Caption: Top: DVS chip with 128x128 pixels, showing zoom preview of 30µm size pixel and schematic on the right, fabricated in AMS 0.35µm. Bottom: Example captures of DVS camera showing high-speed capability, low data-rate (nev is number of events), high intra-scene dynamic range. See ref [A] for details.

phic Group, who coordinated the CAVIAR EU project in which this type of sensor was first invented and exploited. Later on they developed their own prototype which at that time had the best contrast sensitivity, power consumption, and circuit compactness, resulting in 4 licensed patents and the participation in French spin-off company Chronocam, now known as Prophesee.
Main recent activities in this line include:

- Design and fabrication of a number of Dynamic Vision Sensors.

- Improved AER read-out circuitry.

- Design of improved temporal contrast sensitivity prototypes through low power mismatch-insensitive amplification stages.

- Development of new conceptual circuits for alternative operation principles for DVS cameras.

- Low current circuit techniques.

- Fast read-out circuits.

Keywords
Dynamic Vision Sensor; Address Event Representation; Spiking Retinas; Spiking Neural Networks; Asynchronous Circuits; High-Speed Low-Power Vision; DVS Stereo-Vision

Research Highlights

◆ A. Yousefzadeh, G. Orchard, T. Serrano-Gotarredona and B. Linares-Barranco, "Active Perception with Dynamic Vision Sensors. Minimum Saccades with Optimum Recognition", IEEE Transactions on Biomedical Circuits and Systems, vol. 12, no. 4, pp 927-939, 2018

◆ [B] L.A. Camuñas-Mesa, T. Serrano-Gotarredona, S. Ieng, R. Benosman and B. Linares-Barranco, "Event-Driven Stereo Visual Tracking Algorithm to Solve Object Occlusion", IEEE Transactions on Neural Networks and Learning Systems, vol. 29, no. 9, pp 4223-4237, 2017
T. Serrano-Gotarredona and B. Linares-Barranco, "Poker-DVS and MNIST-DVS. Their History, How They were Made, and Other Details", Frontiers in Neuromorphic Engineering, Frontiers in Neuroscience, vol. 9, article 481, 2015

◆ [A] T. Serrano-Gotarredona and B. Linares-Barranco, "A 128x128 1.5% Contrast Sensitivity 0.9% FPN 3µs Latency 4mW Asynchronous Frame-Free Dynamic Vision Sensor Using Transimpedance Amplifiers", IEEE Journal of Solid-State Circuits, vol. 48, no. 3, pp 827-838, 2013

◆ J.A. Leñero-Bardallo, T. Serrano-Gotarredona and B. Linares-Barranco, "A 3.6µs Latency Asynchronous Frame-Free Event-Driven Dynamic-Vision-Sensor", IEEE Journal of Solid-State Circuits, vol. 46, no. 6, pp 1443-1455, 2011

◆ Technology Transfer
Patent: T. Finateu, B. Linares-Barranco, C. Posch and T. Serrano-Gotarredona, "Pixel Circuit for Detecting Time-Dependent Visual Data", WO2018073379A1. Priority 20-Oct-2016. European patent, extended to US, Korea, Japan, China.

◆ Patent: T. Finateu, B. Linares-Barranco, C. Posch and T. Serrano-Gotarredona, "Sample and Hold based Temporal Contrast Vision Sensor", WO2017174579A1. Priority: 4-Apr-2016.

◆ Patent: B. Linares-Barranco and T. Serrano-Gotarredona, "Method and Device for Detecting the Temporal Variation of the Light Intensity in a Matrix of Photosensors", WO2014091040A1. Priority: 11-Dec-2012. European patent, extended to US, Korea, Japan, Israel.

◆ Patent: B. Linares-Barranco and T. Serrano-Gotarredona, "Low-Mismatch and Low-Consumption Transimpedance Gain Circuit for Temporally Differentiating Phot-Sensing systems in dynamic vision Sensors", WO2012160230A1. Priority: 26-May-2011. European patent, extended to US, Korea, Japan, China.

◆ Spin-off Company: Prophesee. Metavision for machines.

Key Research Projects & Contracts

APROVIS3D: Analog PROcessing Of Bioinspired Vision Sensors For 3D Reconstruction
PI: Teresa Serrano Gotarredona
Funding Body: Min. de Ciencia e Innovación
Apr 2020 - March 2023

COGNET: Event-based cognitive vision system. Extension to audio with sensory fusion
PI: Teresa Serrano Gotarredona
Funding Body: Min. de Ciencia e Innovación
Jan 2016 - Dec 2019

ECOMODE: Event-driven compressive vision for multimodal interaction with mobile devices
PI: Bernabé Linares-Barranco
Funding Body: European Union
Jan 2015 - Dec 2018

BIOSENSE: Bioinspired event-based system for sensory fusion and neurocortical processing. High-speed low-cost applications in robotics and automotion.
PI: Teresa Serrano Gotarredona
Funding Body: Min. de Ciencia e Innovación
Jan 2013 - Dec 2015

NANONEURO: Design of neurocortical architectures for vision applications
PI: Teresa Serrano Gotarredona
Funding Body: Junta de Andalucía
Jul 2011 - Dec 2014

RESEARCH AREA ◆ NANOELECTRONICS AND EMERGING TECHNOLOGIES

Circuit Design using Emerging Devices and Non-Conventional Logic Concepts

Contact

José M. Quintana Toledo
josem@imse-cnm.csic.es

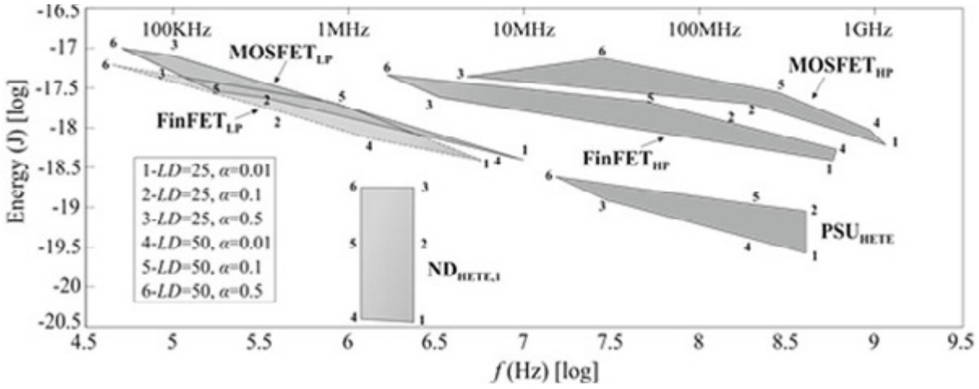
María J. Avedillo de Juan
avedillo@imse-cnm.csic.es

Main research objective is the development, analysis and design of circuits using emerging devices and/or nonconventional logic models, with emphasis on applications with severe constraints on power or energy like IoT. In particular, we explore circuits based on resonant tunel diodes (RTDs), tunel transistors (TFETs and SymFETs) or devices integrating phase transition (Hyper-FETs, VO2). The distinguishing features of these devices is exploited to obtain circuits competitive with respect to their CMOS counterparts in terms of speed, power, energy or area or exhibiting better trade-offs among those criteria. From the logic point of view, we study threshold logic and more recently oscillator-based computing.
Main recent activities in this line include:
- Development of oscillatory neural networks in which the synchronization dynamics of oscillators are used for computation. Oscillators are implemented with a VO2 device and a transistor.

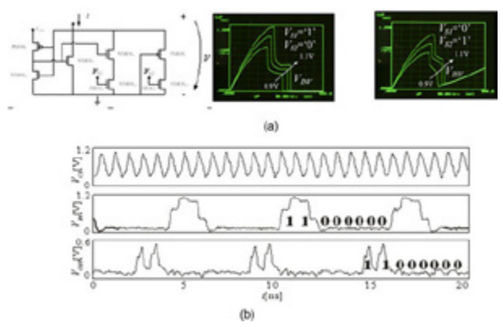
- Development of logic based on the coding of information in the phase of an oscillation. Its main element is an oscillator to which a synchronization signal is injected to discretize its phase. In the case of binary logic, only two phases are used.

- Design and evaluation of logic circuits using TFETs and HyperFETs for low power and energy efficient applications. Technology benchmarlking and identification of application areas, development of gate topologies and logic architectures suitable for the specific characteristics of these devices.

Keywords
Emerging Devices; Coupled Oscillators; Oscillatory



Caption: Evaluation in terms of energy and speed of CMOS transistors (MOSFETs and FinFETs) and tunel transistors (PSUHETE and NDHETE1). Different logic-deths and switching activities are explored.



Caption: a) Programable MOS-NDR exhibiting negative differential resistance; b) Experimental results of a two-phase single-gate-per phase MOBILE pipeline.

Neural Networks; Oscillator-based Computing; VO2; Energy Efficiency; Ultra-Low Power Electronic; Resonant Tunel Diode (RTD); Negative Differential Resistance (NDR); Tunel Transistor (TFET); Steep Subthreshold Slope Devices

Research Highlights

◆ M.J. Avedillo, J.M. Quintana and J. Núñez, "Phase Transition Device for Phase Storing", IEEE Transactions on Nanotechnology, vol. 19, pp 107-112, 2020

◆ M. Jiménez, J. Núñez and M.J. Avedillo, "Hybrid Phase Transition FET Devices for Logic Computation", IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, vol. 6, no. 1, pp 1-8, 2020

◆ J. Núñez and J.M. Avedillo, "Approaching the Design of Energy Recovery Logic Circuits using Tunnel Transistors", IEEE Transactions on Nanotechnology, vol. 19, pp 500-507, 2020

◆ J. Núñez and M.J. Avedillo, "Power and Speed Evaluation of Hyper-FET Circuits", IEEE Access, vol. 7, pp 6724-6732, 2019

◆ J. Nuñez and M.J. Avedillo, "Reducing the Impact of Reverse Currents in Tunnel FET Rectifiers for Energy Harvesting Applications", IEEE Journal of the Electron Devices Society, vol. 5, no. 6, pp. 530-534, 2017

Key Research Projects & Contracts

NEURONN: Two-Dimensional Oscillatory Neural Networks for Energy Efficent Neuromorphic computing (H2020-871501)
PI: Bernabé Linares Barranco
Funding Body: European Union
Jan 2020 - Dec 2022

PULPOSS: Processing for Ultra Low POwer using Steep Slope devices: circuits and arquitectures (TEC2017-87052-P)
PI: María J. Avedillo de Juan / José M. Quintana Toledo
Funding Body: Min. de Economía y Competitividad
Jan 2018 - Dec 2020

NACLUDE: Nano-architectures for logic computing using emergent devices (TEC2013-40670-P)
PI: Jose M. Quintana Toledo / María J. Avedillo de Juan
Funding Body: Min. de Economía y Competitividad
Jan 2014 - Dec 2017

RTDs: Architectures and circuits for logic and non-linear applications using RTDs (TEC2010-18937)
PI: María J. Avedillo de Juan
Funding Body: Min. de Ciencia e Innovación
Jan 2011 - Dec 2014

QUDOS: Quantum Tunneling Device Technology on Silicon (IST-2001-32358)
PI: Werner Prost / WP Coordinator: José M. Quintana Toledo
Funding Body: European Comission
Jan 2002 - Dec 2004

Nanoscale Memristor Circuits and Systems

Contact

Bernabé Linares Barranco
bernabe@imse-cnm.csic.es

Teresa Serrano Gotarredona
terese@imse-cnm.csic.es

Luis A. Camuñas Mesa
camunas@imse-cnm.csic.es

With the end of Moore's Law approaching quickly, mainstream CMOS downscaling is slowing down. Novel nanoscale emerging devices compatible with CMOS fabrication technologies promise to overcome this slow down. Ultra-dense multi-layer fabrics of nano-scale devices can be fabricated as BEOL (back end of line) on top of CMOS substrates. One of these emerging devices are memristors, also called resistive-RAM (RRAM), which are two-terminal devices whose resistance can be changed as the devices are stimulated differently. Some of these memristors allow for two-state resistances, while other less developed may allow for continuous non-volatile analog memory states. In this research line our main focus is to exploit these novel memristive devices combined with optimized CMOS circuits to provide ultra-compact ultra-low-power computing architectures for edge and IoT applications. Main recent activities in this line include:
- Design and fabrication of monolithic CMOS/memristor Proof-of-Concept computing systems using TiO RRAM Filamentary Memristors.

- Computation of Spike-Time-Dependent-Plasticity Learning Rules with Memristors.

- Stochastic Binary Spike-Time-Dependent-Plasticity for Memristor-based 1-bit weight learning and inference.

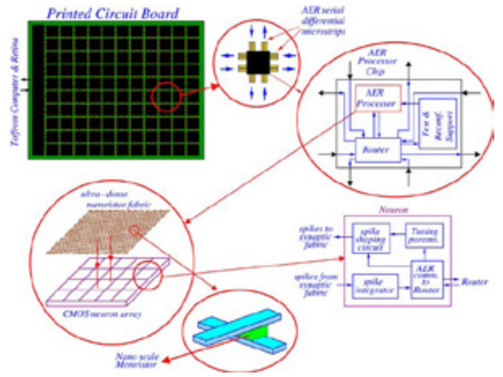
- Calibration Techniques for ultra-low-voltage memristive read-out circuits.

Keywords

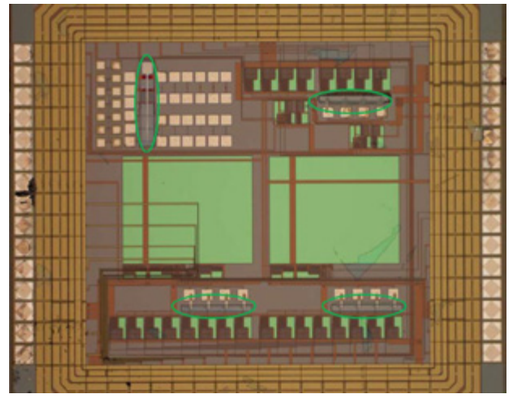
RRAM (Resistive RAM); Non-volatile memristor memory; Nanoscale memristors; TiO filamentary memristors; 1T1R memristor crossbars; Spiking neuromorphic computing with memristors; Hopfield Neural Networks with memristors; Spike-Timing-Dependent-Plasticity with memristors

Research Highlights

◆ L. A. Camuñas-Mesa, B. Linares-Barranco and T. Serrano-Gotarredona, "Neuromorphic Spiking Neural Networks and Their Memristor-CMOS Hardware Implementations", Materials, vol. 12, no. 7, article 2745, 2019



Caption: Illustration of massive computing architectures of monolithic CMOS/Memristor neural computing chips assembled on dedicated PCBs.



Caption: Photograph of CMOS chip with memristor test devices fabricated on top.

B. Linares-Barranco, "Memristors fire away", Nature Electronics, vol. 1, no. 2, pp 100-101, 2018

◆ X. Guo, F. Merrikh-Bayat, L. Gao, B.D. Hoskins, F. Alibart, B. Linares-Barranco, L. Theogarajan, C. Teuscher and D.B. Strukov, "Modeling and Experimental Demonstration of a Hopfield Network Analog-to-Digital Converter with Hybrid CMOS/Memristor Circuits", Frontiers in Neuromorphic Engineering, Frontiers in Neuroscience, vol. 9, article 488, 2015

◆ G. Indiveri, B. Linares-Barranco, R. Legenstein, G. Deligeorgis and T. Prodromakis, "Integration of nanoscale memristor synapses in neuromorphic computing architectures", Nanotechnology, vol. 24, no. 38, article 384010, 2013

◆ C. Zamarreño-Ramos, L. A. Camuñas-Mesa, J.A. Perez-Carrasco, T. Masquelier, T. Serrano-Gotarredona and B. Linares-Barranco, "On Spike-Timing-Dependent-Plasticity, Memristive Devices, and building

a Self-Learning Visual Cortex", Frontiers in Neuromorphic Engineering, Frontiers in Neuroscience, vol. 5, article 26, 2011

Key Research Projects & Contracts

Nano-Mind: Neuromorphic Perception and Nano-Memristive Cognition for High-Speed Robotic Actuation
PI: Teresa Serrano Gotarredona
Funding Body: Min. de Ciencia e Innovación
Jun 2020 - May 2024

MeM-Scales: Memory technologies with multi-scale time constants for neuromorphic architectures
PI: Bernabé Linares Barranco
Funding Body: European Union
Jan 2020 - Dec 2022

HERMES: Hybrid Enhanced Regenerative Medicine Systems
PI: Teresa Serrano Gotarredona
Funding Body: European Union
Jan 2019 - Dec 2022

NeuRAM3: NEUral computing aRchitectures in Advanced Monolithic 3D-VLSI nano-technologies
PI: Teresa Serrano Gotarredona
Funding Body: European Union
Jan 2016 - Jun 2019

MemoCiS: Memristors - Devices, Models, Circuits, Systems and Applications
PI: Bernabé Linares Barranco
Funding Body: COST Action IC1401
May 2014 - May 2018

RESEARCH AREA ◆ BIOMEDICAL AND BIOINSPIRED CIRCUITS AND SYSTEMS

Research Line -> Biomedical Circuits and Systems

Contact

Gloria Huertas Sánchez
gloria@imse-cnm.csic.es

Alberto Yúfera García
yufera@imse-cnm.csic.es

This research line embraces all activities related with the development of alternative bio-instrumentation circuits and systems required to reproduce classical and to propose new measurement techniques at bio-medical labs to improve the quality of acquired biosignals.
Targets design for bio-instrumentation systems are focused also to reduce the human effort and cost of biomedical assays, to obtain the minimum size and weight of biosystems (Lab-on-a-Chips, LoCs), to research new measurement methods based on high performance integrated circuits and system design with low-power consumption, wide bandwidth, reduced power supply levels and wireless communication capability. Electrical modeling of sensors required as signal transducers and interfaces must be incorporated to circuit design flow to obtain full system characterization. This research line also considers the modelling of heterogeneous systems for full system simulations.
Main recent activities are:

- Alternative bio-signals acquisition techniques.
- Development of CMOS circuits and systems blocks.
- To exploit classical sensors and look for new sensor issues for solving biosignals and biomarkers measurement problem.

- Modeling sensor performance and incorporate it into heterogeneous system simulation in a full system design process.

- Development of wearable systems for edema test in heart fail patients.

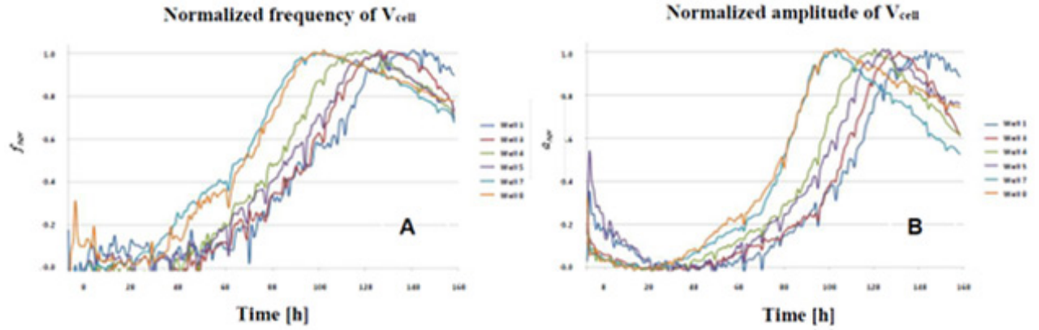
- Electro stimulation of stem cells in differentiation processes.

- Developing multidisciplinary working skills.

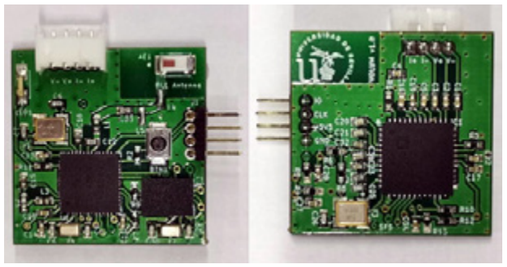
Keywords
Biomedical Circuits and Systems; Bio-Sensors; Laboratory on-a-Chip (LoC); Bioimpedance; Microelectrode; Electro Stimulation (ES); Clinical Applications; Electric Modelling of Biology Systems

Research Highlights

◆ P. Pérez, J.A. Serrano, M.E. Martín, P. Daza, G. Huertas and A. Yúfera, "A computer-aided design tool for biomedical OBT sensor tuning in cell-culture assays", Computer Methods and Programs in Biomedicine, vol. 200, article 105840, 2020



Caption: Normalized frequency (A) and amplitude (B) measured at Vcell in a cell culture. The curves correspond to 2500 cells (W1, W3), 5000 cells (W4, W5) and 10000 cells (W7, W8), seeded at t = 0. Cell proliferation is measured with the oscillation parameters: frequency (fosc) and amplitude (aosc).



Caption: PCB developed for the leg edema test wearable system, to be applied in patients with heart fail disease. The size is set to 2x2 cm2.

◆ J.A. Serrano, P. Pérez, G. Huertas and A. Yúfera, "Alternative general fitting methods for real-time cell-count experimental data processing", IEEE Sensors Journal, vol. 20, no. 24, 2020

◆ P. Pérez, G. Huertas, A. Maldonado-Jacobi, M. Martín, J.A. Serrano, A. Olmo, P. Daza and A. Yúfera, "Sensing Cell-Culture Assays with Low-Cost Circuitry", Scientific Reports, Nature Group, vol. 8, article 8841, 2018

◆ D. Rivas-Marchena, A. Olmo, J.A. Miguel, M. Martinez, G. Huertas and A. Yufera, "Real-time electrical bioimpedance characterization of neointimal tissue for stent applications", Sensors, vol. 17, no. 8, art. 1737, 2017

◆ G. Huertas, A. Maldonado, A. Yufera, A. Rueda and J.L. Huertas, "The Bio-Oscillator: A Circuit for Cell-Culture Assays", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 62, pp. 164-168, 2015

◆ Technology Transfer
Gloria Huertas Sánchez, Andrés Maldonado Jacobi and Alberto Yúfera García. Bioimpedance measurement system for wirelessly monitoring cell cultures in real time, based on an oscillation test using integrated circuits. 2014

◆ Alberto Yúfera García, Alberto Olmo Fernández and Gloria Huertas Sánchez. Bioimpedance measuring system for wirelessly monitoring cell cultures in real time, based on CMOS circuits and electrical modelling. 2014

Key Research Projects & Contracts

SYMAS: Sistema de medida y electroestimulación para aplicaciones de diferenciación y motilidad celular (P18-FR-2308)
PI: Alberto Yúfera García / Gloria Huertas Sánchez
Funding Body: Junta de Andalucía - Proyectos de Excelencia
Jan 2020 - Dec 2022

VOLUM: Valor pronóstico en tiempo real para la monitorización del volumen mediante medidas de bioimpedancias en pacientes con insuficiencia cardíaca aguda (HEART-FAIL VOLUM)
PI: Alberto Yúfera García
Funding Body: Instituto de Salud Carlos III
Jan 2020 - Dec 2021

iSTENT: Real Time Monitoring of Hemodinamic Variables using Smart Stents (iSTENT) based on Capacitive and Bioimpedance Sensors (RTI2018-093512-B-C21)
PI: Alberto Yúfera García
Funding Body: Min. de Ciencia e Innovación
Jan 2019 - Dec 2021

MIXCELL: Integrated MicroSystems for Cell-Culture Assays
PI: Alberto Yúfera García
Funding Body: Min. de Economía y Competitividad
Jan 2014 - Dec 2017

ACATEX: Self-calibration and self-test of analog, mixed-signal and radio frecuency circuits (P09-TIC-5386)
PI: Adoración Rueda Rueda
Funding Body: Junta de Andalucía - Proyectos de Excelencia
Mar 2010 - Feb 2014

Research Line -> Wireless Implantable and Wearable Intelligent Biosensor Devices

Contact

Manuel Delgado Restituto
mandel@imse-cnm.csic.es

Research on bioengineering including integrated sensing/read-out circuitry for the detection and recording of neural signals, wearable electronic devices for healthcare monitoring, and efficient wireless interfaces for intelligent medical devices (IMD). The common denominator to these research lines is the need to achieve high precision, low-noise analog read-out and very low power dissipation, in order to enable solutions which can be powered through small-capacity batteries and/or harvesting techniques.
Different activities are being developed in this area:

- Definition of enabling technologies for the integration and miniaturization of biomimetic systems, which can be used for building neurocortical implants suitable for scientific (to allow new advances in neuroscience), clinical (to provide neuroprosthesis for the treatment of neurological diseases), and translational application (to pave the way for brain-machine interfaces) issues.

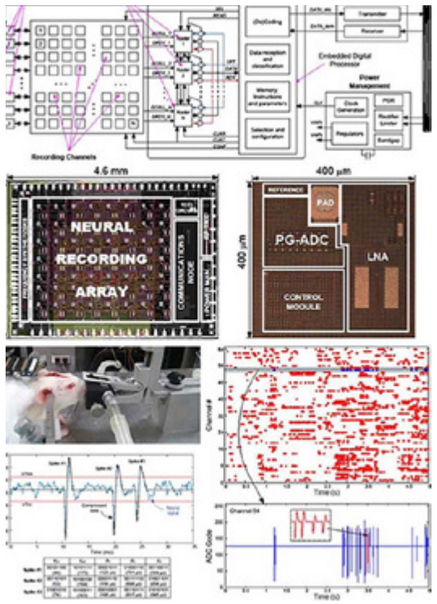
- Development of novel neurological data processing algorithms, including data compression, artifact suppression and seizure prediction processors, suitable for closed-loop therapeutic systems for refractory epilepsy and movement disorder diseases.

- Implementation of wireless sensor nodes (WSN) to quantify the impairments of the neuromuscular function and movement observed in Parkinson disease patients including means of surface electromyography (EMG) or kinematic measurements.

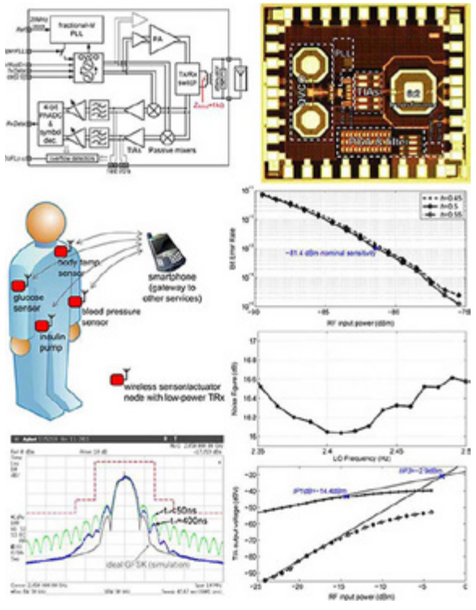
- Fabrication of passive radio-frequency identification (RFID) biomedical sensor tags, including mechanisms for remotely powering, suitable for the acquisition and conditioning of biomedical signals such as body temperature, blood glucose level or ECG information.

- Design of standard-compliant transceivers for wireless body area network (WBAN) applications, including novel architectures and circuit techniques for phase domain modulation.
More details can be found in www2.imse-cnm.csic.es/~mandel/

Keywords
Biomedical Circuits and Systems; Neuro-Engineering; Low-Noise Sensor Readout; Low-Power Wireless Interfaces; Telemetry Systems; Energy Harvesting



Caption: Fully implantable multichannel cortical neural recording system and experimental verification in vivo with animal model.



Caption: Ultra-low power transceiver for Bluetooth Low Energy (BLE). The receiver (Rx) skips any active RF stage and it is implemented as a passive front-end. It achieves a sensitivity of -81.4 dBm and consumes less than 1.1 mW. The transmitter employs direct modulation and an efficient class-E power amplifier (PA) to deliver 1.6 dBm output power to the antenna with a total efficiency of 24.5%.

Research Highlights

◆ R. Fiorelli, M. Delgado-Restituto and Á. Rodríguez-Vázquez, "Charge-Redistribution Based Quadratic Operators for Neural Feature Extraction", IEEE Transactions on Biomedical Circuits and Systems, vol. 14, no. 3, pp. 606-619, 2020

◆ J. L. Valtierra, M. Delgado-Restituto, R. Fiorelli and Á. Rodríguez-Vázquez, "A Sub-µW Reconfigurable Front-End for Invasive Neural Recording that Exploits the Spectral Characteristics of the Wideband Neural Signal", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 5, pp. 1426-1437, 2020

◆ R. Fiorelli, M. Delgado-Restituto and Á. Rodríguez-Vázquez, "Offset-Calibration with Time-Domain Comparators using Inversion-Mode Varactors", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 1, pp. 47-51, 2020

◆ M. Delgado-Restituto, J. B. Romaine and Á. Rodríguez-Vázquez, "Phase Synchronization Operator for On-Chip Brain Functional Connectivity Computation", IEEE Transactions on Biomedical Circuits and Systems, vol. 13, no. 5, pp. 957-970, 2019

◆ M. Delgado-Restituto, A. Rodríguez-Pérez, A. Darie, C. Soto-Sánchez, E. Fernández-Jover and Á. Rodríguez-Vázquez, "System-Level Design of a 64-Channel Low Power Neural Spike Recording Sensor", IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 2, pp. 420-433, 2017

Key Research Projects & Contracts

MIRABRAS: Millimeter-sized Implant with embedded Responsive Artificial intelligence for Brain disorder Assistance (PID2019-110410RB-I00)
PI: Manuel Delgado Restituto
Funding Body: Min. de Ciencia, Innovación y Universidades
Jan 2020 - Dec 2022

IPANEMA: Integrated Pattern-Adaptive optical NEurostimulator with Multi-site recording Array (TEC2016-80923-P)
PI: Manuel Delgado Restituto
Funding Body: Min. de Economía, Industria y Competitividad
Jan 2017 - Dec 2019

CLEPSYDRA: Towards a Closed-Loop Epileptogenic Prediction SYstem based on sub-Dural Recording Arrays (TEC2012-33634)
PI: Manuel Delgado Restituto
Funding Body: Min. de Economía y Competitividad
Jan 2013 - Dec 2015

POWDERS: Ultra-Low Power Wireless Motes for the Remote Sensing of Biomedical Signals (TEC2009-08447)
PI: Manuel Delgado Restituto
Funding Body: Min. de Ciencia e Innovación
Jan 2010 - Dec 2012

BIO-TAG: Monolithic Implementation of Passive RFID Transponders for Biomedical Applications (TIC-02818)
PI: Manuel Delgado Restituto
Funding Body: Junta de Andalucía
Dec 2007 - Dec 2011

RESEARCH AREA ◆ INTEGRATED CIRCUITS FOR SPACE APPLICATIONS

Research Line -> High-Speed High-Resolution ADCs & DACs for Space Applications

Contact

Gildas Léger
leger@imse-cnm.csic.es

Antonio J. Ginés Arteaga
gines@imse-cnm.csic.es

This line of research addresses the design of analog and mixed-signal circuits and systems for critical aerospace applications, with emphasis on embedded aerospace applications (satellites, rovers) in CMOS (Complementary Metal-Oxide Semiconductor) technology. These circuits are characterized by being in an environment with high doses of radiation (TID, SE) and need for an autonomous operation without maintenance.
In order to increase the performance and increase the lifespan of these systems, it is necessary to develop and implement Radiation-Hard (Rad-Hard) techniques. In addition and, especially in an application context with little or no possibility of human intervention, these systems should include additional circuitry that capable of automatically measuring and correcting (self-calibration) errors by itself during the entire life of the Instrument (due to the cumulative effect of radiation and aging, as well as change of PVT operating conditions: process, voltage and temperature).
The advantages of research and development of self-calibration techniques are of great importance in

critical applications operating under extreme conditions, since the performance of the circuits subjected to stress tend to degrade over time, requiring periodic re-calibrations to preserve the specified operating level.
Another aspect to emphasize is the reliability and reuse of this type of circuits, once developed and qualified, for future missions, which entails a great savings in terms of effort and associated costs.

Keywords
Auto-Calibration; Hardness for Radiation Applications; Embedded Critical Aerospace Applications (Satellites, Rovers, etc.); Sensors; Temperature Sensors; Solar Irradiance Sensors; Mixed Signal ASICs-CMOS for Space

Research Highlights

◆ A.J. Ginés, E.J. Peralías and A. Rueda, "Black-Box Calibration for ADCs With Hard Nonlinear Errors Using a Novel INL-Based Additive Code: A Pipeline ADC Case Study", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 7, pp. 1718-1729, 2017

◆ J. Núñez, A.J. Ginés, E.J. Peralías and A. Rueda, "Design methodology for low-jitter differential clock recovery circuits in high performance ADCs", Analog Integrated Circuits and Signal Processing, vol. 89, no. 33, pp. 593-609, 2016

◆ A.J. Ginés, E. Peralías and A. Rueda, "Background Digital Calibration of Comparator Offsets in Pipeline ADCs" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 7, pp. 1345-1349, 2015

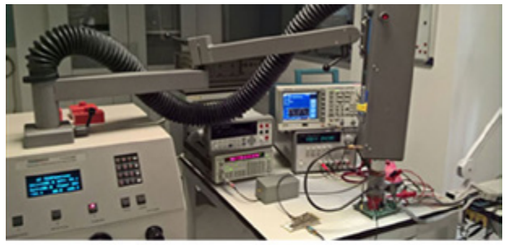
◆ D. Malagon-Perianez, J.M. de la Rosa, R. del Rio and G. Leger, "Single Event Transients trigger instability in Sigma-Delta Modulators", Conference on Design of Circuits and Integrated Systems (DCIS), Madrid, 2014

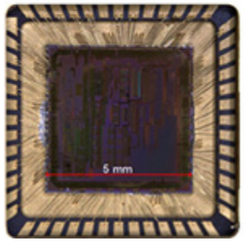
◆ J. Ramos-Martos, A. Arias-Drake, A. Ragel-Morales, J. Ceballos-Cáceres, J.M. Mora-Gutiérrez, B. Piñero-García, M. Muñoz-Díaz, M.A. Lagos-Florido, S. Espejo-Meana, I. Arruego-Rodríguez, J. Martínez-Oter and M.T. Álvarez, "OWLs: A Mixed-Signal ASIC for Optical Wire-Less Links in Space Instruments", Fourth International Workshop on Analog and Mixed-Signal Integrated Circuits for Space Applications, AMICSA, ESA/ESTEC, Noordwijk, The Netherlands, 2012

Key Research Projects & Contracts

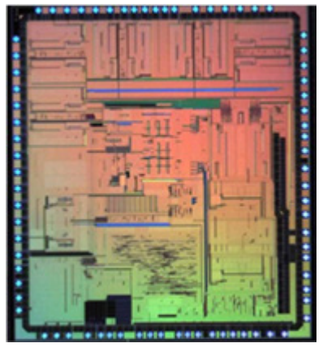
ASIC-SIS: ASIC for compacts solar irradiation sensor (ESP2016-80320-C2-2-R)
PI: Diego Vázquez García de la Vega
Funding Body: Min. de Economía, Industria y Competitividad
Dec 2016 - Dec 2018

16BitADC (ESA ITT AO/1-7154 /12/NL/RA)





Caption: Test assembly for evaluation of electrical behavior at extreme temperatures. Front microphotograph of the CMOS prototype of the 16bitADC converter.



Caption: Photograph of ASIC CMOS 0.35µm Front-End for solar irradiation sensors on the surface of Mars. The circuit has been designed with the rad-hard library (hardened against radiations) developed at the Microelectronics Institute of Seville (IMSE-CSIC-US).

PI: Juan Ramos (up to 08/2015) / Joaquín Ceballos / Antonio Ginés (from 09/2015)
Funding Body: ESA (European Space Agency)
Sep 2013 - Dec 2015

DANTE: Adapting Mixed-signal and RF ICs Design and Test to Process and Evironment Variability (TEC2011-28302)
PI: Adoración Rueda Rueda
Funding Body: Min. de Ciencia e Innovación
Jan 2012 - Dec 2015

Radiation Tolerant Analogue/Mixed-Signal Technology Survey and Test Vehicle Design (ESTEC Contract No. 400010162110/NL/AF)
PI: José Luis Huertas / Gildas Léger
Funding Body: ESA (European Space Agency) - Through subcontract with ARQUIMEA
Sep 2010 - Sep 2012

Research Line -> System-on-Chip ASICs for Space Instrumentation

Contact

Servando Espejo Meana
espejo@imse-cnm.csic.es

Joaquín Ceballos Cáceres
joaquin@imse-cnm.csic.es

This line is devoted to the development of integrated circuits and analog/mixed-signal systems for space applications, and in general, for applications in environments suffering radiation and extreme temperatures, with high reliability requirements. The use of conventional CMOS technologies is emphasized, following the concept of radiation hardening by design (RHBD).
Specific activities include the characterization of the effects of high-energy electromagnetic and particles radiation (total ionizing dose –TID, and single-event effects -SEE) on integrated circuit production technologies, on devices and circuits, and the development of robust strategies for the design of circuits and systems. Other topics of interest include the tolerance of circuits to extended temperature ranges, and the resistance of packages and systems to thermal cycles, impacts, and vibration.
Accomplished tasks include:
- Characterization of a 0.35µm CMOS technology concerning radiation effects and extended temperature ranges.

- Development of radiation tolerant digital-cells libraries.

- Development of electrical models for the simulation of MOS transistors with specific radiation-hardened layouts (ELTs).

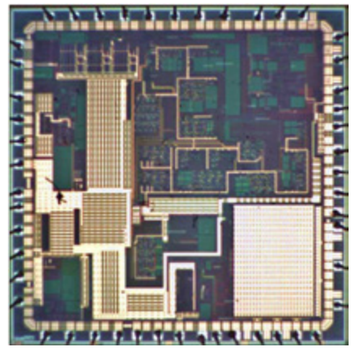
- Design and test of several mixed-signal ASICs for space use.
  · OWLS: intra-satellite optical communications based on diffuse light.
  · MOURA: tri-axial magnetometer and accelerometer.
  · MEDA: wind sensor for MEDA, for Mars'2020.
  · SIS: solar irradiance sensor for Exomars'18.

- Formal qualification processes for the space-use of mixed-signal ASICs.

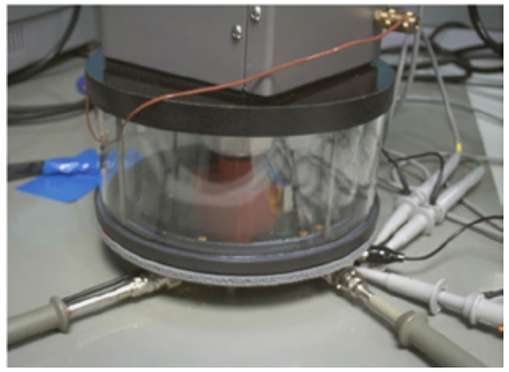
Keywords
Radiation Hardening; Extended Temperature Ranges; Reliability; Total Ionizing Dose; Single-Event Effects; Redundancy; Latch-up Prevention

Research Highlights

◆ S. Sordo-Ibáñez, B. Piñero-García, M. Muñoz-Díaz, A. Ragel-Morales, J. Ceballos-Cáceres, L. Carranza-González, S. Espejo-Meana, A. Arias-Drake, J. Ramos-Martos, J.M. Mora-Gutiérrez and M.A. Lagos-Florido, "CMOS Rad-Hard Front-End Electronics for Precise Sensors Measurements", IEEE Transactions on Nuclear Science, vol. 63, pp. 2379-2389, 2016



Caption: ASIC OWLS



Caption: ASIC for MEDA wind sensor

◆ S. Sordo-Ibáñez, B. Piñero-García, M. Muñoz-Díaz, A. Ragel-Morales, J. Ceballos-Cáceres, L. Carranza-González, S. Espejo-Meana, A. Arias-Drake, J. Ramos-Martos, J.M. Mora-Gutiérrez and M.A. Lagos-Florido, "A Front-End ASIC for a 3-D Magnetometer for Space Applications by Using Anisotropic Magnetoresistors", IEEE Transactions on Magnetics, vol. 51, pp. 1-4, 2015

◆ S. Sordo-Ibáñez, S. Espejo-Meana, B. Piñero-García, A. Ragel-Morales, J. Ceballos-Cáceres, M. Muñoz-Díaz, L. Carranza-González, A. Arias-Drake, J.M. Mora-Gutiérrez, M.A. Lagos-Florido and J. Ramos-Martos, "Four-channel self-compensating single-slope ADC for space environments", Electronics Letters, vol. 50, pp. 579-581, 2014

◆ J. Ramos-Martos, A. Arias-Drake, J.M. Mora-Gutiérrez, M. Muñoz-Díaz, A. Ragel-Morales, B. Piñero-García, J. Ceballos-Cáceres, L. Carranza-González, S. Sor-

do-Ibáñez, M.A. Lagos- Florido and S. Espejo-Meana, "SEE Characterization of the AMS 0.35 µm CMOS Technology", in Proc. of the 14th European Conf. on Radiation and its Effects on Components and Systems, pp. 1-4, 2013

◆ J. Ramos-Martos, A. Arias-Drake, A. Ragel-Morales, J. Ceballos-Caceres, J.M. Mora-Gutierrez, B. Pinero-Garcia, M. Munoz-Diaz, M.A. Lagos-Florido and S. Espejo-Meana, "Radiation Characterization of the austriamicrosystems 0.35 µm CMOS Technology", in Proc. of the 12th European Conf. on Radiation and its Effects on Components and Systems, 2011

Key Research Projects & Contracts

Microelectrónica para instrumentación espacial: ASIC del sensor de viento de MEDA (ESP2016-79612-C3-3-R)
PI: Servando Espejo Meana
Funding Body: Min. Economía y Competitividad
Jan 2017 - Dec 2018

Microelectrónica de espacio para instrumentación ambiental en Marte (ESP2014-54256-C4-4-R)
PI: Servando Espejo Meana
Funding Body: Min. Economía y Competitividad
Jan 2015 - Dec 2015

Diseño y testado de ASICs para el espacio para la misión a Marte 'MEIGA-METNET Precursor' (AYA2011-29967-C05-05)
PI: Servando Espejo Meana
Funding Body: Min. de Ciencia e Innovación
Jan 2012 - Dec 2012

Diseño y testado de ASICs para el espacio para la misión a Marte 'MEIGA-METNET Precursor' (AYA2009-14212-C05-04)
PI: Servando Espejo Meana
Funding Body: Min. de Ciencia e Innovación
Jan 2010 - Dec 2011

Diseño y testado de ASICs para el espacio para la misión a Marte 'MEIGA-METNET Precursor' (AYA2008-06420-C04-02/ESP)
PI: Servando Espejo Meana
Funding Body: Min. de Ciencia e Innovación
Jan 2009 - Dec 2009

RESEARCH AREA ◆ HARDWARE SECURITY

Cybersecurity

Contact

Iluminada Baturone Castillo
lumi@imse-cnm.csic.es

Carlos J. Jiménez Fernández
cjesus@imse-cnm.csic.es

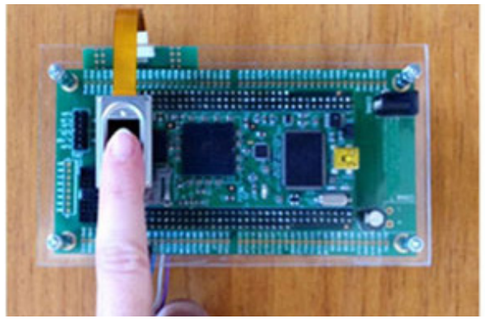
This research line focuses on microelectronic solutions for security applications. The objectives are to verify the identity of hardware devices and users as well as to store and communicate sensitive information, resorting to the use of techniques from cryptography, biometrics, and their combination (crypto-biometrics). Security against hardware attacks is especially analyzed, particularly fault injection and side-channel attacks such as differential power analysis (DPA) and differential electromagnetic attacks (DEMA). Microelectronic solutions are aimed at constructions and algorithms providing security together with efficient features of size, power consumption and operation speed.
The activities within this research line are devoted to:
- Exploration of cryptographic algorithms from a secure hardware implementation point of view. Development of architectures for such algorithms with optimized features in terms of VLSI design and resistance against attacks.
- Analysis of side-channel and fault-injection attack sources. Development of robust hardware solutions as well as setups and benchmarks to measure the security of microelectronic realizations against attacks. Vulnerability metrics.

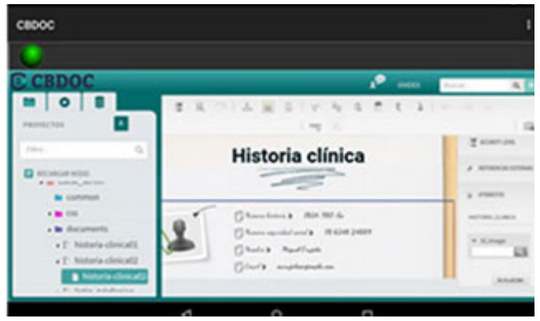
- Design of modules based on PUFs (within programmable devices and/or integrated circuits) to implement security primitives particularly related to key generation, identifiers, and random numbers.

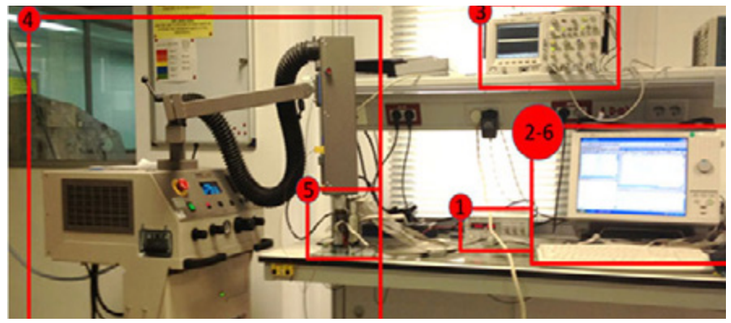
- Hardware implementation of algorithms to process and recognize biometric features such as fingerprints, faces, gait, voice, etc. Design of microelectronic solutions for biometric, multi-biometric, and crypto-biometric systems.

- Application of the above solutions to wearable devices, tokens, tags, consumer electronic devices, control systems, etc.

Keywords
Hardware for Cryptography; Biometrics and Crypto-Biometrics; Physical Unclonable Functions (PUFs); Secure FPGAs and Integrated Circuits; Hardware Attacks; Authentication and Secure Communications







Caption: Prototype of e-padlock which allows dual-factor authentication (what you have and who you are) in the access to a content management system.

Caption: Experimental setup to measure hardware security: 1.- Power supply, 2.- Logic analyzer, 3.-Osciloscope, 4.- Temperature control system, 5.- Device under test, 6.- Software to automate measurements.

Research Highlights

◆ J.M. Mora-Gutiérrez, C.J. Jiménez-Fernández and M. Valencia-Barrero, "Trivium Hardware Implementations for Power Reduction", International Journal of Circuit Theory and Applications, Special Issue: Secure lightweight crypto-hardware, vol. 45, no. 2, pp. 188-198, 2017

◆ A. Cabrera-Aldaya, A.J. Cabrera and S. Sánchez-Solano, "SPA Vulnerabilities of the Binary Extended Euclidean Algorithm", Journal of Cryptographic Engineering, vol 7, no. 4, pp. 273-285, 2017

◆ I. Baturone, M.A. Prada-Delgado and S. Eiroa, "Improved generation of identifiers, secret keys, and random numbers from SRAMs", IEEE Transactions on Information Forensics and Security, vol. 10, no. 12, pp. 2653-2668, 2015

◆ E. Tena-Sánchez, J. Castro and A.J. Acosta, "A Methodology for Optimized Design of Secure Differential Logic Gates for DPA Resistant Circuits", IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 4, no. 2, pp 203-215, 2014

◆ R. Arjona and I. Baturone, "A Hardware Solution for Real-Time Intelligent Fingerprint Acquisition", Journal of Real-Time Image Processing, vol. 9, no. 1, pp. 95-109, 2014

Key Research Projects & Contracts

INTERVALO: Integración y validación en laboratorio de contramedidas frente a ataques laterales en criptocircuitos microelectrónicos (TEC2016-80549-R)
PI: Antonio J. Acosta Jiménez / Carlos J. Jiménez Fernández
Funding Body: Min. de Economía y Competitividad
Dec 2016 - Dec 2019

SENIAC: Security in interconnected devices by injection of authentication and ciphering algorithms (RTC-2014-2932-8)
PI: Iluminada Baturone Castillo
Funding Body: Min. de Economía y Competitividad
Oct 2014 - Mar 2017

CESAR: Secure microelectronic circuits against side-channel attacks (TEC2013-45523-R)
PI: Antonio J. Acosta Jiménez / Carlos J. Jiménez Fernández
Funding Body: Min. de Economía y Competitividad
Jan 2014 - Dec 2016

CB-DOC: Content management system with secure authentication by cripto-biometric techniques based on hardware (IPT-2012-0695-390000)
PI: Iluminada Baturone Castillo
Funding Body: Min. de Economía y Competitividad · Proyecto INNPACTO
Jul 2012 - Mar 2015

CRIPTO-BIO: Microelectronic design for crypto-biometric authentication (P08-TIC-03674)
PI: Iluminada Baturone Castillo
Funding Body: Junta de Andalucía - Proyectos de Excelencia
Jan 2009 - Dec 2013

Security and Reliability in CMOS and Emerging Technologies

Contact

Francisco V. Fernández Fernández
pacov@imse-cnm.csic.es

The development of IoT in the near future faces numerous technological challenges that need to be addressed, such as power/energy efficiency, reliability, security, and cost. Advanced CMOS technologies are potential candidates for solutions in the short term to those challenges, whereas beyond-CMOS devices are the answer for solutions in the long term. All these technologies are plagued with both time-zero and time-dependent variability effects. From a reliability point of view, design strategies and methodologies are required to deal with the mitigation or tolerance to variability effects. But from an exploitation perspective, variability can be regarded as an advantage rather than as a problem, e.g. in the hardware security field.
This research line focusses in the development of new and robust Physical Unclonable Functions and lightweight cryptographic solutions combining the experience of researchers in reliability characterization and reliability-aware design in CMOS technology and low-power circuit design in beyond-CMOS technologies. More specifically, the work includes activities in the following design areas:
- Design of Physical Unclonable Functions: Exploitation of time-zero and time-dependent variability effects in microelectronic devices for security applications.
- Reliability
  · Characterization and modeling of time-zero and time-dependent variability effects in micro/nano-electronic devices.
  · Robustness of lightweight cryptographic solutions.
- Low-power circuit design in beyond-CMOS technologies.

Keywords
Hardware Security; PUF; Lightweight Cryptography; Reliability; Variability Effects; Beyond-CMOS Devices

Research Highlights

◆ P. Saraza-Canflanca, H. Carrasco-Lopez, A. Santana-Andreo, P. Brox, R. Castro-Lopez, E. Roca and F.V. Fernandez, "Improving the reliability of SRAM-based PUFs under varying operation conditions and aging degradation", Microelectronics Reliability, vol. 118, article 114049, 2021.

◆ P. Saraza-Canflanca, J. Martin-Martinez, R. Castro-Lopez, E. Roca, R. Rodriguez, F.V. Fernández and M. Nafria, "Statistical characterization of time-dependent variability defects using the máximum current fluctuation", IEEE Transactions on Electron Devices, vol. 68, no. 8, pp 4039-4044, 2021

◆ J. Díaz-Fortuny, P. Saraza-Canflanca, R. Castro-Lopez, E. Roca, J. Martin-Martinez, R. Rodriguez, F.V. Fernández and M. Nafria, "Flexible Setup for the Measurement of CMOS Time-Dependent Variability with Array-Based Integrated Circuits", IEEE Transactions on Instrumentation and Measurement, vol. 69, no. 2, pp 853-864, 2020

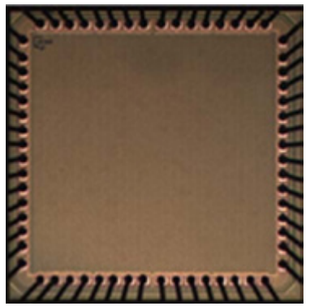
◆ I.M. Delgado-Lozano, E.Tena-Sánchez, J. Núñez and A. Acosta, "Design and analysis of secure emerging crypto-hardware using HyperFET devices", IEEE Transactions on Emerging Topics in Computing, vol. 9, no. 2, pp 787-796, 2020

◆ J. Diaz-Fortuny, J. Martin-Martinez, R. Rodriguez, R. Castro-Lopez, E. Roca, X. Aragonés, E. Barajas, D. Mateo, F.V. Fernandez and M. Nafria, "A Versatile CMOS Transistor Array IC for the Statistical Characterization of Time-Zero Variability, RTN, BTI and HCI", IEEE Journal of Solid-State Circuits, vol. 54, no. 2, pp 476-488, 2019

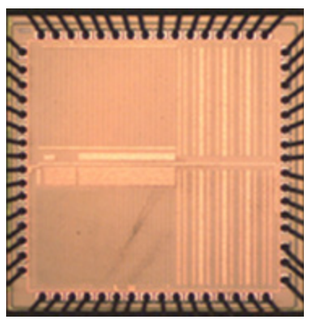
Key Research Projects & Contracts

VIGILANT: The Variability Challenge in Nano-CMOS - SUB-PROJECT MITIGATION (PID2019-103869RB-C31)
PI: Francisco V. Fernández Fernández / Rafael Castro López
Funding Body: Min. de Ciencia, Innovación y Universidades
Jun 2020 - May 2023

TOGETHER: Towards Trusted Low-Power Things: Devices, Circuits and Architectures (TEC2016-75151-C3-3-R)
PI: Francisco V. Fernández Fernández / Rafael Castro López
Funding Body: Min. de Economía, Industria y Competitividad
Jan 2017 - Jun 2021



Caption: ENDURANCE: Chip design for the statistical characterization of time-dependent variability at device level. It includes four large arrays of CMOS transistors.



Caption: KIPT: Chip design for the statistical characterization of time-dependent variability at circuit level. It includes four large arrays of cells or circuit blocks: one array of SRAM and Sense Amplifier, one array of Analog Circuits and two of Ring Oscillators.

FOUNDED PROJECTS

EU PROJECTS

- SPINAGE
- HERMES
- SPIRS
- ARTURO
- HEROIC
- CROSSBRAIN
- GOIT
- NIMBLE AI
- PEROSPIKER
- QUBIP
- SQPRIM
- ARCHYTAS

NATIONAL PROJECTS

- CORDION
- VIGILANT
- NANO-MEM
- ARES
- HARDWALLET
- AEROSKIN
- E-CELL
- FEMPS
- SEMIOTICS
- LIFELINE
- ULTIMATE
- VIPS-ID
- SMARTRANS
- RADIAN
- SIP-SEXI
- TIRELESS
- EUPHORIC
- ELIXIR
- HIGHLOAWALLET
- MEMVIS
- SARATSO
- AIR CHIP
- ASIC-IMTER
- HARD ID WALLET
- DIGISOLAR F2
- DEDOSS
- RISC-V
- USECHIP

REGIONAL PROJECTS

- BIOVEO
- RTN SECURE

CSIC PROJECTS

- DEEP-MAX-IMSE PHASE 1
- I-COOP 2022
- ELEVATE
- TECHNOQUANTUM
- DORAITO
- MOMENTUM BLB
- INTRAMURAL ECOIMSE-IND
- INTRAMURAL SETIT
- INTRAMURAL CONTADOR
- AYUDAS INCORPORACIÓN CIENTÍFICOS TITULARES 2024
- AYUDAS IMOVE

INTERNATIONAL AND OTHER TYPES OF PROJECTS

- MEM2CNN
- HEART-FAIL

CONTRACTS

- REMOTE MONITORING FOR BIRD SPECIES IDENTIFICATION IN SEO/BIRDLIFE MONITORING PROGRAMS
- TECHNICAL CONSULTING FOR THE DEVELOPMENT OF INTEGRATED CIRCUITS OF EMBEDDED SYSTEMS IN THE FIELD OF SECURITY
- DEVELOPMENT AND PREPARATION OF CYBERSECURITY VERIFICATION METHODOLOGIES IN INTEGRATED CIRCUITS (SOC AND SIP)
- DESIGN AND DEVELOPMENT OF FIRMWARE FOR SMART IMAGE CAPTURE DEVICES
- STUDY ON THE AUTOMATIC IDENTIFICATION OF BIRD SPECIES IN SEO/BIRDLIFE MONITORING PROGRAMS
- DESIGN OF INNOVATIVE CHIPS FOR THE FIRST HIGH-PERFORMANCE, LOW-POWER MULTIFUNCTIONAL INTEGRATED BOARD IN STRATOSPHERIC BALLOONS (CHIP-NESE)
- MINIATURIZED SENSOR FOR LONG TERM MONITORING OF ATOMIC OXYGEN DEGRADATION PROCESSES IN VLEO MISSIONS
- SUPPORT FOR THE STUDY OF THE APPLICATION OF PULSED LASER TECHNIQUE FOR SCREENING AND CHARACTERIZATION OF ELECTRONIC COMPONENTS FOR SPACE APPLICATIONS
- RESEARCH ON SIMSIDES BLOCKSET
- DESIGN OF RECONFIGURABLE MICROELECTRONIC CIRCUITS
- CONTRACT FOR TECHNICAL CONSULTING FOR THE DEVELOPMENT OF INTEGRATED CIRCUITS FOR SECURITY APPLICATIONS

EU PROJECTS

SPINAGE

Weighted Spintronic-Nano-Oscillator-based Neuromorphic Computing System Assisted by laser for Cognitive Computing

PI: **Teresa Serrano Gotarredona**

Projects Details:
Type: **Research Project**
Funding Body: **European Union**
Reference: **H2020-FETOPEN-2020-01-899559**
Start date: 01/09/2020 End date: **31/08/2024**
Funding: **437.577,x00 €**

The brain is a highly complex, high performance and low energy computing system due to its massive parallelism and intertwined network, which outperforms the current computers by orders of magnitudes, especially for cognitive computing applications. A large effort has been made into understanding the computing and mimicking the brain into an artificial implementation, so-called neuromorphic computing that has received much attention thanks to the advances in novel nanoscale technologies. The current implementation of the neuromorphic computing systems (NCS) using Complementary Metal-Oxide-Semiconductor (CMOS) technologies has 5-6 orders of magnitude lower performance (operation/sec/Watt/cm3) compared to the brain. Spintronic devices, using the spin of the electron instead of its charge, have been considered one of the most promising approaches for implementing not only memories but also NCSs leading to a high density, high speed, and energyefficiency. The main goal of SpinAge is to realize a novel NCS enabling large-scale development of braininspired devices outclassing the performance of current computing machines.

This will be achieved by the novel structures using spintronics and memristors, on-chip laser technology, nano electronics and finally advanced integration of all these technologies. We expect this unprecedented combination of emerging technologies will lead to at least 4-5 orders of magnitude better performance than the state-of-the-art CMOS-based NCSs. The approach taken in SpinAge is to implement synaptic neurons using novel nanoscale weighted spin-based nanooscillators, assisted by a low-energy laser pulse irradiation from an integrated plasmonic laser chip, integrated all with the CMOS interfacing electronics for a proof-of-concept of a 16x16 NCS for cognitive computing applications. Our breakthrough platform technology will demonstrate EU leadership of advanced neuromorphic computing.

HERMES

Hybrid Enhanced Regenerative Medicine Systems.

PI: **Teresa Serrano Gotarredona**

Projects Details:
Type: **Research project**
Funding Body: **European Union**
Reference: **H2020-FET-PROACT-2018-01-824164**
Start date: 2019/ End date: **2023**
Funding: **438.511,25 €**

Brain disorders are the most invalidating condition, exceeding HIV, cancer and heart ischemia, with significant impact on society and public health. Regenerative medicine is a promising branch of health science that aims at restoring brain function by rebuilding brain tissue. However, repairing the brain is one of the hardest challenges and we are still unable to effectively rebuild brain matter. Epilepsy is particularly challenging due to its dynamic nature caused by the relentless brain damage and aberrant rearrangements of brain rewiring. To overcome the biological uncertainty of canonical regenerative approaches, we propose an innovative solution based on intelligent biohybrids, made by the symbiotic integration of bioengineered brain tissue, neuromorphic microelectronics and artificial intelligence, to effectively drive self-repair of dysfunctional brain circuits and we validate it against animal models of epilepsy. HERMES fosters the emergence of a novel biomedical paradigm, rooted in the use of biohybrid neuronics (neural electronics), which we name enhanced regenerative medicine.

To this end, HERMES will promote interdisciplinary cross-fertilization within and outside the consortium; it will extend the concepts of enhanced brain regeneration to philosophy, ethics, policy and society to foster the emergence of a new innovation eco-system. Intelligent biohybrids will represent a major breakthrough to advance brain repair research beyond regenerative medicine and neurotechnology alone; it will bring new knowledge in neurobiology, cognitive neuroscience and philosophy, and new neuromorphic technology and AI algorithms. HERMES will bring a giant conceptual leap that will shift the concept of biomedical interventions from treating to healing. In turn, it will potentially generate major returns on health care and society at large by bringing previously unimaginable possibilities to defeat disorders that represent today a global major burden of disease.

SPIRS

Secure Platform for ICT Systems Rooted at the Silicon Manufacturing Process.

PI: **Piedad Brox Jiménez**

Projects Details:
Type: **Research project**
Funding Body: **European Union**
Reference: **952622**
Start date: 01/10/2021 End date: **30/09/2024**
Funding: **610.028,25 €**

Our society is continuously demanding more and more intelligent devices, along with network infrastructures and distributed services that make our daily lives more comfortably. However, the frantic adoption of Internet of Things (IoT) technologies has led to widespread implementations without a deep analysis about security matters.

This project encompasses the complete design of a platform, so-called SPIRS platform, which integrates a hardware dedicated Root of Trust (RoT) and a processor core with the capability of offering a full suite of security services. Furthermore, the SPIRS platform will be able to leverage this capability to support privacy-respectful attestation mechanisms and enable trusted communication channels across 5G infrastructures.

RoT is implemented in hardware with a dedicated circuitry to extract a unique digital identifier for the SPIRS platform during its entire lifetime. To build a complete solution, the project also features a Trusted Execution Environment (TEE), secure boot, and runtime integrity. Furthermore, resilience and privacy protection are major concerns in this project, and it endeavors to the design of a decentralized trust management framework targeted to minimize the impact of Single Point of Failure (SPOF) risks and achieve adequate security and privacy tradeoffs. To facilitate the tasks of validation and testing, SPIRS platform is conceived as an open platform that can easily integrate other building blocks and facilities upgrades.

The project goes beyond the construction of the SPIRS platform and it provides solutions to integrate it in the deployment of cryptographic protocols and network infrastructures in a trustworthy way, leveraging the RoT provided by the platform.

To validate SPIRS results, the project considers two different scenarios: Industry 4.0 and 5G Technologies.

ARTURO

Advanced Radar Technologies in eUROpe.

PI: **Ángel Rodríguez Vázquez**

Projects Details:
Type: **Research project**
Funding Body: **European Defence Fund (EDF)**
Reference: **101074813**
Start date: 01/01/2023 End date: **31/12/2025**
Funding: **401.792,50 €**

The ARTURO (Advanced Radar Technologies in eUROpe) project proposes a solution to fulfil future operational needs based on extended use of emerging technologies. More specifically, studies of ARTURO project will be focused on:

1. Representing end-users vision in terms of needs and high-level requirements for the future most demanding scenarios and environments;

2. Defining an innovative Sensor Architecture and the most efficient applicable technologies to be implemented in the future development,

3. In-depth analysis of the new threats and the environment surrounding the radar which produces an accurate definition of the various operational scenarios (air, land and naval) the new class of radar is expected to cope with;

4. Carrying out the study of modern HW (hardware) and SW (software) technologies that provide the constituent elements of the new class of radar. New approaches to design (i.e. cognitive) and modern technologies such as Artificial Intelligence will be disseminated within the design;

5. Supporting the above topics by selecting a specific preliminary development of key components of the new architecture;

6. Proposing a roadmap for future developments based on the results derived by the current research

HEROIC

High Efficiency Read Out Circuits.

PI: **Ángel Rodríguez Vázquez**

Projects Details:
Type: **Research project**
Funding Body: **European Defence Fund (EDF)**
Reference: **101102939**
Start date: 01/01/2023 End date: **31/12/2026**
Funding: **771.625,00 €**

Many defence applications rely on Infrared (IR) optronics systems to detect, recognise, and identify objects or targets during night and day. These systems are composed of IR sensors able to detect electromagnetic radiation within a wavelength spectrum different from the visible one. At the heart of the IR sensor lies the Focal Plane Array, broken down into two functional layers, the detection layer and the Read-Out Integrated Circuit (ROIC). The key features of a ROIC are to provide the electrical interface between each individual detector pixel and its associated readout circuit and to convert the signals provided by the pixel readout circuit into a digital equivalent that can be provided to the sensor output and acquired by the external driving electronics. Currently the mainstream sizes of IR sensors for defence applications are between VGA (640 x 480 pixels) format and SXGA format (1280 x 1024 pixels) and pixel pitch distance between 20 µm and 10 µm.

The next generations of IR systems will require longer detection, recognition and identification ranges, large field of views, faster frame rates and higher performance. At IR sensor level, this calls for larger formats and reduction of the pixel pitch distance to typically ≤7,5µm so as not to physically increase the size of the sensor and thus maintain acceptable system costs and mechanical/electrical interfaces. The qualification of a more advanced Complementary-metal-oxide-semiconductor (CMOS) technology is mandatory. The HEROIC ambition is to enable European IR sensor suppliers to sustainably design the next generation of EU ROICs for IR sensors for defence applications. HEROIC unites, from across EU, different complementary players in the supply chain, including key system manufacturers and IR technology providers. HEROIC represents a first phase in the securing of the availability of a common advanced fully EU ROIC supply chain compatible with various IR detector technologies and 2D/3D architectures by 2030.

CROSSBRAIN

Distributed and federated cross-modality actuation through advanced nanomaterials and neuromorphic learning.

PI: **Bernabé Linares Barranco**

Projects Details:
Type: **Research project**
Funding Body: **European Union**
Reference: **101070908**
Start date: 01/11/2022 End date: **31/12/2026**
Funding: **402.905,00 €**

A vast number of pathological brain conditions directly involve aberrant electrical activity of the brain. CROSSBRAIN centres its technological revolution on the convergence of novel nanoactuation modalities, bleeding-edge nano-electronics, and miniaturized wireless energy harvesting and communication. Combining extreme edge computing with advanced nanomaterials featuring tailored physical properties, biocompatible coatings, and material modifications to prevent glial scarring, CROSSBRAIN will enable individualized, adaptive and highly spatiotemporally localized actuation of brain tissue. It will leverage sensing electric local field potentials, multiunit neuronal activity, and cross-modal nanomaterial-based modulation (electrical, mechanical, thermal, ionic concentration, optogenetics) of neuronal excitability with on-board intelligence. The CROSSBRAIN platform comprises a swarm of wireless, implantable, MRI-compatible microbots for in vivo electrophysiology and cross-modal neuromodulation at the cell- and microcircuit levels, in freely moving rodents. CROSSBRAIN delivers a multiplicity of stimulation modalities, involving electro-mechano-magneto-thermo-optical principles for modulation of nerve cell excitability.

The microbots will feature both sensing and actuation electrodes, engineered with nanomaterials and viral vectors coatings. They will be implanted endovascularly, deliver genetic material upon command, and operate in federation under the networked control and wireless power supply by a tiny central unit, which can be worn like an internet of things device. CROSSBRAIN will deliver autonomous or manual, closed-loop sensing, prediction, and actuation through combining multiple neuromodulation mechanisms, which will act in a synergistic and dynamic manner to optimally shape stimulation according to individual neuronal firing patterns or clinician's needs. As case studies, we will explore CROSSBRAIN action in animal models of Parkinson's Disease and Epilepsy.

GOIT

Go IT!

PI: **Piedad Brox Jiménez**

Projects Details:
Type: **Research project**
Funding Body: **European Union**
Reference: **101070660**
Start date: 01/09/2022 End date: **31/08/2025**
Funding: **167.236,60 €**

Europe's IT hardware development is constantly challenged by outrageously expensive development tools, legal constraints like NDAs or patents, lock-in threats, dependency from external vendors or supply chains and foreign political events. Europe's digital infrastructure (from consumer to critical appliances) is heavily relying on foreign closed-source chips which are literally black-boxes which may (and have been proven to) contain malicious features. This situation makes the hardware development expensive and inefficient, and undermines the very principle of sovereignty, resilience and re-usability.

Open-source silicon chips, which are open in their entirety, i.e. down to the physical layout, carry the potential of catapulting Europe into a renaissance of digital technology. Several challenges are on the way, many of which will require the participation of the stakeholders (from the fertile ground made of "nerdy" hobbyists and makers who are the early protagonists of the scene, all the way up to large enterprises), as well as the participation of policymakers and regulatory bodies. The road ahead is steep, but rich of rewards. Therefore, we loudly say: Go IT!

NIMBLE AI

Ultra-energy efficient and secure neuromorphic sensing and processing at the endpoint.

PI: **Bernabé Linares Barranco**

Projects Details:
Type: **Research project**
Funding Body: **European Union**
Reference: **101070679**
Start date: 01/10/2022 End date: **30/09/2025**
Funding: **740.740,00 €**

Today only very light AI processing tasks are executed in ubiquitous IoT endpoint devices, where sensor data are generated and access to energy is usually constrained. However, this approach is not scalable and results in high penalties in terms of security, privacy, cost, energy consumption, and latency as data need to travel from endpoint devices to remote processing systems such as data centres. Inefficiencies are especially evident in energy consumption. To keep up pace with the exponentially growing amount of data (e.g., video) and allow more advanced, accurate, safe and timely interactions with the surrounding environment, next-generation endpoint devices will need to run AI algorithms (e.g., computer vision) and other compute intense tasks with very low latency (i.e., units of ms or less) and energy envelops (i.e., tens of mW or less). NimbleAI will harness the latest advances in microelectronics and integrated circuit technology to create an integral neuromorphic sensing-processing solution to efficiently run accurate and diverse computer vision algorithms in resource- and area-constrained chips destined to endpoint devices.

Biology will be a major source of inspiration in NimbleAI, especially with a focus to reproduce adaptivity and experience-induced plasticity that allow biological structures to continuously become more efficient in processing dynamic visual stimuli. NimbleAI is expected to allow significant improvements compared to state-of-the-art (e.g., commercially available neuromorphic chips), and at least 100x improvement in energy efficiency and 50x shorter latency compared to state-of-the-practice (e.g., CPU/GPU/NPU/TPUs processing frame-based video). NimbleAI will also take a holistic approach for ensuring safety and security at different architecture levels, including silicon level.

PEROSPIKER

Perovskite Spiking Neurons for Intelligent Networks

PI: **Bernabé Linares Barranco**

Projects Details:
Type: **Research project**
Funding Body: **European Union**
Reference: **101097688**
Start date: 01/10/2023 End date: **30/09/2028**
Funding: **100.000,00 €**

A brain is a complex structure where computing and memory are tightly intertwined at very low power cost of operation, by analog signals across vast quantities of synapse-connected spiking neurons. Animal brains react intelligently to environmental events and perceptions. By developing similar Spiking Neural Networks (SNN) we can realize neuromorphic computation systems excellent for dealing with large amounts of noisy data and stimuli and very well suited for perception, cognition and motor tasks. But the current CMOS technologies perform very poorly for emulating the biological brains and their power consumption is large. Currently we cannot replicate biological neurons behaviours with existing design and manufacturing techno-

logy. This project aims to develop compact miniature material elements that will emulate closely the complex dynamic behaviour of neurons and synapses, to form SNNs with substantial reduction in footprint, complexity and energy cost for perception, learning and computation. We investigate the properties of metal halide perovskite that have produced excellent photovoltaic devices in the last decade.

These perovskites have ionic/electronic conduction, hysteresis, memory effect and switchable and nonlinear behaviour, that make them ideally suited for the realization of devices in close fidelity to biological electrochemically gated membranes in neurons, and information-tracking synapses. We will use the methodology of impedance spectroscopy and equivalent circuit analysis to fabricate devices with dynamic responses emulating the natural neuronal coupling and synchronization. This method will produce the hardware that we need for a preferred spiking computational model, incorporating time, analog physical elements and dynamical complexity as computational tools. As illustration we will show visual object recognition from spiking data provided by a spiking retina by advanced neuristors and dynamic synapses.

QUBIP

Quantum-oriented Update to Browsers and Infrastructures for the PQ Transition.

PI: **Piedad Brox Jiménez**

Projects Details:
Type: **Research project**
Funding Body: **European Unio**n
Reference: **101119746**
Start date: 01/09/2023 End date: **31/08/2026**
Funding: **303.721,00 €**

The exciting frontiers opened by the development of quantum computers (QC) come at the cost of breaking the foundations of current digital security. The research community is working to the definition of post-quantum cryptography (PQC) to counteract this threat. However, the transition to PQC is delicate and takes time because it impacts many functions, algorithms, and protocols in a-priori unknown cascade of dependencies. QUBIP is conceived to contribute to the EU transition to PQC with the goal of simplifying and making replicable the process by means of recommended practices and counteract post-quantum threats as soon as possible. QUBIP focuses on digital infrastructure addressing the 5 main building blocks that use public-key cryptography for security purposes: hardware, cryptographic libraries, operating system, communication protocols and applications. QUBIP address all 5 blocks coherently solving all dependency issues that may arise inside each block and among blocks with the final aim to validate at TRL6 three infrastructures making use of those blocks in IoT-based Digital Manufacturing, Internet Browsing, and Software Networks Environments for Telcos use cases.

The return-of-experience from the three practical exercises is then maximized by developing a migration playbook, that will contain the lessons learned and an evaluation of all the technical, economic, and legal barriers encountered together with the solutions to overcome them to enable the definition of a replicable process, suitable to provide structured accompanying and practical guidance to industrial stakeholders. The technical activities are corroborated by three supporting activities (i) evaluation of the capabilities of QCs to assess their implication to primitives, algorithms and protocols adopted, and contribution to (ii) standardization efforts addressing transition to PQC processes and (iii) policy measures addressing technology changes coming from the advent of QC and PQC.

SQPRIM

Secure post-quantum cryptographic primitives.

PI: **Piedad Brox Jiménez**

Projects Details:
Type: **Research project**
Funding Body: **European Union**
Reference: **101105985**
Start date: 01/07/2023 End date: **30/06/2025**
Funding: **181.152,96 €**

Quantum computers pose a huge threat to cybersecurity, with the potential of solving complex problems in just a fraction of the time it takes to the most powerful supercomputers today. With conventional public key infrastructure (PKI) cryptography at risk, we face the task of securing our digital systems with the development of new cryptographic primitives for the post-quantum era. Inspired by nature, this project aims to developing the biometric equivalents of fingerprints and DNA for the digital world that will univocally and individually identify hardware. For this goal, Physically Unclonable Functions (PUFs) will be developed to provide hardware-based digital identifiers that will be utilised to build lightweight encryption and robust authentication procedures. But creating such unique structures is challenging in a fast-growing digital environment with increasing demand for new interconnected devices, such as the Internet of Things (IoT).

To achieve this goal, we will combine light and sound. We will use ultrasound (US) waves to control the travel path of a light beam transmitted through a scattering medium to generate unique patterns. This novel method can potentially generate a high number of unique patterns while reducing the cost and complexity compared to current systems exploiting optical PUFs. The proposed device is expected to be unconditionally unclonable and, therefore, safe in the post-quantum era.

This project will also explore the integration of the proposed novel PUFs with CMOS-based cryptographic primitives to create IDentity of Things (IDoT). The proposed solution is expected to be of relevance in a wide spectrum of application domains such as financial systems, medical services, energy industry, governments, and citizens.

ARCHYTAS

ARCHitectures based on unconventional accelerators for dependable/energY efficienT AI Systems

PI: **BERNABÉ LINARES BARRANCO**

Projects Details Type
Funding Body: **European Defence Fund (EDF)**
Reference: **101167870**
Start date: 01/12/2024 End date: **30/07/2027**
Funding: **755.371,67 €**

The project aims to investigate and study the feasibility of non-conventional AI accelerators for defence applications that take advantage of novel technologies at the device and package level, such as optoelectronic-based accelerators, volatile and non-volatile processing-in-memory, and neuromorphic devices. The project distinctly addresses the challenges encountered in the defence use cases by proposing optimised solutions for efficient energy consumption, speed, and cost.

LICORICE

reLIable and sCalable tOols foR self-sovereIgn identity and data proteCtion framEwork

PI: **ILUMINADA BATURONE CASTILLO**

Projects Details
Type: **Research project**
Funding Body: **European Union**
Reference: **101168311**
Start date: 01/10/2024 End date: **30/09/2027**
Funding: **284.625,00 €**

Global accelerated digital transformation, shaped by disruptive technologies (AI and Big Data, Metaverses and Web3, etc.), brings both unprecedented opportunities for EU citizens and businesses and emerging and increased challenges: surge in sophisticated cyber-attacks, multifarious forms of data abuse and the corresponding growth of public concern over loss of data control or identity-related crimes. In this context, preserving trust among stakeholders with strong data protection guarantees is vital for digital services delivery in more secure online environments which benefit from the upcoming EU Digital Identity ecosystem and for fully developing EU data spaces for data exchange in federated computation scenarios.

With its results accurately oriented towards Digital Decade's cardinal points and target areas, fully aligned with EU's Digital Identity and Data Strategy, directly contributing to strengthening EU's digital and data sovereignty and also complementing outcomes from EUDI Wallet Large Scale Pilots, LICORICE Innovation Action delivers 2 highly-advanced, reliable and trustworthy self-sovereign identity and privacy-preserving toolsets for user-centric, cryptographically secure identity management and verifiable federated data sharing and computing. They will align with latest EUDI Wallets specifications and data space blueprints, models and frameworks to deliver high scalability and efficiency, also featuring usability and ease-of-adoption (including by SMEs), with solid open source strategy oriented to large developer communities and boosting commercial exploitation by its industrial partners. Results will be fully validated over 2 iterations of piloting, demonstrating integration of toolset prototypes in operational environments of two high-impact pilots in domains of Cyber Threat Intelligence AI-based assistance and sharing, and eHealth services and biomedical research. LICORICE has 12 partners from 8 EU Member States and a 36-month duration.

NATIONAL PROJECTS

CORDION

Digitizers based on Cognitive Radio for IoT nodes.

PI: **José M. de la Rosa Utrera**

Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovación**
Reference: **PID2019-103876RB-I00**
Start date: 01/06/2020 End date: **31/07/2024**
Funding: **55.902,00 €**

IoT (Internet of Things) implies the interconnec- tion of billions of cyberphysical entities, capable of communicating with each other, without the need lor human intervention, also relerred to machine- to-machine communication. However, the practi- cal implementation of IoT requires also the deve- lopment of electronic devices that are secure and efficient in terms of cost and energy consumption. They also need to be equipped with a certain level of intelligence giving rise lo the so-called smart de- vices/objects and autonomy, so that they can make decisions in real time, and locally, i.e. withoul being connected to remate servers.

The so-called Cognitive Radio (CR) technology allows communication systems to make a more efficient use of the electromagnetic spectrum, by dynamically modifying its transmission and re- ception parameters according to the information sansed from the environment a technique also re- ferred to as spectrum sensing. One of the direct consequences of the physical implementations of CR-based terminals is that the digitizers, i.e. the circuits responsible for transforming the signal from the analog to the digital domain, should be placed as clase as possible to the antenna, so that most of the hardware is digital and hence, it is easier to program vía software.

Another key technology enabler for the develop-ment of CR-based IoT nodes is the need to embed a certain degree of Artificial Intelligence (AI), so that they can set their specifications in an optimum and autonomous way, according to the environment conditions (communication coverage, spectrum oc- cupancy, intereferences), battery status and energy consumption.

In this scenario, this project aims to address some of the design challenges for the increased in-coming digital-driven world directly linked to the Economía, Sociedad y Cultura Digitales, which is one of the priority challenges of the Plan Estatal 2017- 2020. To this end, AI-managed digitizers for CR-based IoT nodes will be developed in this project.

VIGILANT

The Variability Challenge in Nano-CMOS: From Device Modeling to IC Design for Mitigation and Exploitation.

PI: **Francisco V. Fernández Fernández, Rafael Castro López**

Projects Details:
Type: **Research project**
Funding Body: **Agencia Estatal de Investigación (AEI) n**
Reference: **PID2019-103869RB-C31**
Start date: 01/06/2020 End date: **29/02/2024**
Funding: **117.491,00 €**

Electronic devices flood many aspects of our lives. The wondrous evolution of nano-CMOS technologies with the emergence of new materials and devices is behind it. The demand for integrated circuits (ICs) is not without challenges though: our modern digital economy and society requires them to be more functional, more reliable, safer and more secure, and fields like IoT, Cybersecurity and Highperformance computing are now priorities in many research agendas.

However, one critical obstacle in this evolution is variability, culprit for the device parametric fluctuations deriving in a reliability loss of the IC. Rising right after fabrication (TZV, Time-Zero Variability) or during the IC lifetime (TDV, Time-Dependent Variability), it ends up critically compromising its functionality or even cutting short its lifetime. If variability is undealt with, ICs will no longer be able to fulfil the capabilities of safety, security, and reliability.

VIGILANT faces up this challenge from two perspectives. It will first develop solutions and new design paradigms to lessen or tolerate variability; the goal is clear: mitigate its negative impact. Second, realizing variability has also a beneficial side, TZV and TDV will be exploited for hardware-based security. While this duality mitigation/exploitation is one key goal, there is another cross-cutting goal: the evaluation of several technologies and their potential for the duality, from the established bulk CMOS, through the versatile FD-SOI, to beyond-CMOS alternatives like memristors. To undertake the goals, VIGILANT needs the complementary expertise of teams (IMSE, UAB and UPC) with a successful track record in the collaborative investigation of variability.

NANO-MIND

Neuromorphic Perception and NANO-Memristive CognItioN for High-SpeeD Robotic Actuation.

PI: **Teresa Serrano Gotarredonao**

Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovación**
Reference: **PID 2019-105556GB**
Start date: 01/06/2020 End date: **31/05/2024**
Funding: **208.770,00 €**

In the last years, due to the availability of large amounts of annotated data and the increase of the computation capability of highperformance computing platforms, we have witnessed a resurgence of artificial intelligence (AI) and neuro-inspired computation. AI systems outperforming human beings in image classification tasks have been demonstrated. However, those systems still lag well behind human beings if we compare them in terms of speed and energy efficiency. The intensive computation requirements of AI recognition systems cause that the developed AI systems for our portable devices perform computations on the cloud. It has been foreseen that by the year 2025, one-fifth of the world's electricity will be consumed by the internet.
The development of efficient information coding schemes and low power AI hardware platforms is a must if we want to witness the spreadof AI systems while keeping an affordable energy budget. Current state-of-the-art AI systems are based on an information coding and processing paradigm which is quite different from the way biological brains code and process the information. If we consider vision as an example, state-of-the-art AI computational vision systems code and process the information as sequences of static frames.

However, biological neurons produce and communicate sequences of spikes. In this context, the so-called third generation of neural networks or spiking neural networks has emerged to emulate the efficiency in information coding and computation of human brains. However, spiking neural networks computational systems lack the maturity of frame-based conventional computing systems in terms of theoretical development, learning and controlling algorithms and availability of event-based sensors, event-based hardware computing platforms, and event-based robotic actuators.

The NANO-MIND project aims to advance in the theoretical and hardware development of neuromorphic spiking neural systems from the sensors level, to the processing level up to the control and actuation level.

ARES

Design, implementation and validation of attack-resistant hardware roots of trust for secure embedded systems.

PI: **Carlos Jesús Jiménez**

Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovación**
Ref: **PID2020-116664RBI00**
Start date: 01/09/2021 End date: **31/08/2025**
Funding: **146.410,00 €**

The inclusion of secure elements in embedded devices is improving in current available commercial solutions. Some manufacturers offer solutions to protect their products against cybersecurity threats. However, the restricted hardware resources of certain devices (e.g. in the Internet-of-Things context) make unfeasible the adoption of some of these complex protection schemes such as Trusted Platform Modules. The design of a Root-of-Trust (RoT) using low-cost hardware modules is presented in this project as alternative. The RoT is conceived as cornerstone, thus deriving trust for the rest of components that compose the embedded system. The RoT will be designed to be a modular, configurable and adaptable structure, thus leveraging the resources to offer dedicated solutions for each particular application case.

The tendency of open source initiatives for embedded systems has been consolidated with the advent and rapid growth of the RISC-V Instruction Set Architecture (ISA) together with its comprehensive hardware and software ecosystems. However, the open nature of RISC-V ISA is a double edged-sword for security purposes. The flexibility of the instruction set allows the possibility of developing various cryptography-specific extensions or variants of the ISA with the aim of increasing the level of security.

But at the same time, the full-access to many 'open-hardware' implementations of the RISC-V ISA could expose them to more vulnerabilities compared to the proprietary world where this information is hidden and protected by strong Intellectual Property rights. Therefore, the development of solutions to foster the security of embedded systems based on this ISA is an open challenge for research community. This project will increase the security of embedded RISC-V systems by incorporating a RoT anchored in the device's own hardware. This strategy will be also adapted to be used by cores with proprietary

ISA, thus allowing to establish a performance comparison between both choices (open and non-open) for embedded systems.

The general objective of the ARES project is to provide hardware solutions to improve the security of embedded systems, designing a hardware RoT that includes cryptographic primitives for secure storage, processing and transmission of data. The building components of the RoT will be Physical Unclonable Functions (PUFs) to generate the identity of the electronic device and generate cryptographic keys as well as entropy sources, and cryptographic primitives for data encryption and decryption. All these elements will include measures to verify its correct behavior and countermeasures to prevent physical attacks. Implementations will be carried out in both FPGA and ASIC technology, using ARM and RISC-V processors, suitable to be used in Internet-of-Things (IoT) technology. For the sake of validation, the project will develop a demonstrator to leverage project advances in a sector as eHealth where security is crucial.

HARDWALLET

Trusted, Post-Quantum Secure Hardware for Decentralized Identity Wallets Using Distinctive Traits of People and Devices.

PI: **Iluminada Baturone / Mª del Rosario Arjona**

Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovación**
Ref: **PID2020-119397RB-I00**
Start date: 01/09/2021 End date: **30/08/2024**
Funding: **83.853,00 €**

Electronic identification allows entities to prove electronically that they are who they say they are in order to access services and carry out electronic transactions. Identity verification uses identifiers, which are uniquely associated with entities, and verification mechanisms that prove the association between the entity and its identifiers. In decentralized identity systems, entities have complete control of their identifiers. Entities are the owners and issuers of their identity (there are no centralized registries, no identity providers, no certification authorities to assign identities as centralized and federated systems do).

Distributed ledger technology, including blockchains, or some other form of decentralized network, enables identity verification using cryptography. Currently, the most established method for verification employs digital signatures. The entity is the only one that has a private key associated with a public key. The most secure solution locally generates its own private and public key pair so that the private key is truly private. Therefore, the genuine entity is the only one capable of generating signatures with its private key and any other entity can verify the signatures with the public key. The decentralized network stores public identifiers and public keys, The current W3C draft on Decentralized IDentifiers (DIDs) includes verification mechanisms, such as public keys and pseudonymous biometrics, that the owner can use to prove their association with the DID. However, most applications verify an individual by applying biometrics locally. No external verifier can prove that the individual actually participates in the process. The reason is that practical and efficient implementations of pseudonym biometrics that offer irreversibility, unlinkability and revocability are still a challenge in decentralized networks.

The HardWallet Project will address the challenge of verifying pseudonymous biometrics externally, meeting demand from Europe and the United States for a decentralized and better privacy-preserving approach. As the IoT and artificial intelligence are producing more and more autonomous electronic devices that conduct electronic transactions as an individual, the HardWallet project will extend verification externally to physical devices with unique electronic characteristics using PUFs (Physical Unclonable Functions). cloneable).

Nowadays, the hardware solutions used in digital wallets to manage private keys and guarantee the integrity of the platform, the confidentiality of the data stored in a non-volatile memory and the authenticity of the executed code (in charge of locally verifying the biometric data sensitive) use classical cryptography. The HardWallet Project will develop secure and reliable hardware to also generate pseudonyms from biometrics and device metrics. In addition, to guarantee long-term security, the cryptography used in the wallet will be post-quantum.

AEROSKIN

Intelligent skin for airflow monitoring.

PI: **Servando Espejo Meana**

Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovación**
Ref: **CPP-2021-008740**
Start date: 01/09/2022 End date: **31/08/2025**
Funding: **52.366,00 €**

AEROSKIN (Smart Skin for Airflow Sensing) is a project that aims to unlock the ability to monitor airflow at multiple locations in a non-intrusive way, a key technology in multiple applications such as optimising aircraft flight efficiency, improving power generation in wind turbines or monitoring the health of structures exposed to airflow.

Smart Skin is a flexible and non-intrusive structure capable of measuring locally at multiple points the characteristics of the airflow simultaneously, instead of providing the information at a macroscopic level as is currently done. This technology is critical for the development of aircraft that adapt their shape during flight, which is one of the pillars to be developed to meet the EU's ambitious targets for reducing fuel consumption and emissions in the aerospace industry.

Building on the legacy of three instruments developed by a consortium member (UPC) used in NASA Mars missions (REMS (Rover Environmental Monitoring Station) for Mars Science Laboratory mission, TWINS for InSight and MEDA (Mars Environment Dynamics Analyzer) for Mars2020), the AEROSKIN team proposes to develop a scaled prototype of a wing equipped with 'Smart Skin' to be tested in a medium-sized wind tunnel, with the aim of demonstrating its capabilities in a controlled environment, thus increasing the Technology Maturity Level (TRL) to 4 as a first step to bring this solution to the aeronautical and energy markets.

E-CELL

Optimization of differentiation processes in stem and tumour cells based on electrostimulation.

PI: **Alberto Yúfera García**

Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovación**
Ref: **PID2021-122529OB-I00**
Start date: 01/09/2022 End date: **31/08/2025**
Funding: **152.944,00 €**

It is proposed to carry out embedded Electronic Systems (ES) for the supervision and characterization of cells and cell cultures, which allow to act on them by means of programmable electrostimulation signals (EST). The objective is to study, know and improve the techniques of cell differentiation towards various types of lineages and tissues of interest in regenerative medicine. The design and manufacture of systems with reduced weight and size, energy autonomous and wireless are pursued, which reduce the workload, automate experiments and monitor in real time the evolution of a cell culture based on electrical BioImpedance (BI) as a marker. It is proposed to monitor the evolution of neuroblastoma, breast cancer, lung cancer, myoblast and osteoblast cell lines, useful in regenerative therapies, tissue engineering, and cancer research, towards the conformation of the corresponding cell or tissue type, optimizing the differentiation processes through design of the adequate signals of electrical stimulation. From the results obtained in a first measurement setup, two more setups are proposed: one oriented to the clinical development of tissue engineering; and another dedicated to the study and characterization of EST processes at the cellular level, through the manufacture of microelectrode arrays (MicroElectrode Array, MEA).

Taking advantage of this last setup, we propose its application in cancer studies, in two aspects: on the one hand, evaluating the effect of EST as a tumou0r inhibitory technique (in the N2A and SK-N-SH lines), and on the one hand, another, using MEAs for the determination of cell motility: position and velocity of tumour cells in cultures (A-549 and MCF7). In summary, monitoring SEs and ESTs measuring electrical BIs will be developed, in parallel to a cell and tissue biometry procedure for the real-time identification of the biological material differentiated or not, and its dynamic characteristics: position, trajectory and speed, with application in tissue engineering and cancer. The results will be validated using biomedical experimentation standards in the proposed cell lines.

FEMPS

Front-End Microelectronics for Planetary Sensors.

PI: **Servando Espejo Meana**

Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovación**
Ref: **PID2021-126719OB-C43**
Start date: 01/01/2022 End date: **31/12/2024**
Funding: **151.250,00 €**

The FEMPS project has four specific objectives. The first one is to contribute and support the integration, calibration and qualification for space of the new spherical wind sensor developed by the Polytechnic University of Catalonia, which is an evolved version of the previous MEDA wind sensor, currently on Mars. The spherical wind sensor uses a mixed-signal ASIC designed using "radiation hardening by design techniques", which performs the conditioning, acquisition and conversion of the sensor signals. This ASIC was developed by the research team under previous projects.

The second objective is the design, at the architectural level, of a new mixed-signal ASIC for a new sensor (Subsurface 3D Heat Flux), whose concept has also been developed by the Polytechnic University of Catalonia. The critical analog front-end blocks will be designed and verified, eliminating feasibility uncertainties, and leaving the ASIC in a semi-finished sta-

te, pending only the definition of digital aspects that may be specific for specific missions (interphase, configurability), and the exhaustive functional verification of the complete system before its submission to foundry. The third objective is the exploration of opportunities and circuitry requirements for a set of chemical and biological sensors, defined by the Center of Astrobiology.

Finally, the fourth objective, related to the second, is the characterization for space use of the high voltage, high power devices available in the selected integrated circuit fabrication process. These devices are necessary in a multitude of sensing systems, including the one foreseen in the second objective. Having them characterized is a strategic positioning for future developments. Radiation effects (total ionizing dose and singular events) and very low temperature effects will be characterized.

SEMIoTICS

Embedded intelligence in low-power vision sensors and systems for robust and autonomous long-term operation.

PI: **Ricardo Carmona Galán /Jorge Fernández Berni**

Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovació**n
Ref: **PID2021-1280090B-C31**
Start date: 01/09/2022 End date: **31/08/2025**
Funding: **212.234,00 €**

The main objective of this project is to provide IoT devices with energy-efficient machine vision-based intelligence by integrating advanced sensing capabilities and algorithms adapted to these capabilities. Today, convolutional neural networks (CNNs) have become the underlying processing architecture for many vision-related tasks. Although their accuracy is much higher than that of classical vision algorithms based on manually designed feature extraction (in fact, this is the main reason for the high relevance of CNNs), the hardware and energy resources they require are massive.

This is mainly due to the fact that the input data stream of such neural networks consists of a serialisation of the raw information provided by the sensor (at most, this information previously goes through a specific processor for image enhancement: edge enhancement, tone mapping, etc.). We intend to explore different alternatives to incorporate vision into embedded platforms in a much more efficient way. We will start by addressing the problem of reliable generation of scene representations in all kinds of situations. Thus, we will study high dynamic range techniques based on the operation of natural systems (in particular the retina) to accommodate extreme lighting conditions in a signal range equivalent to 8 bits. This will involve computational relief from the very beginning of the signal chain. At the pixel level, we will look for an operation based on the interaction of two diodes that will provide each other with information about the local and global illumination in the scene at each instant. The tasks to be performed will range from physical modelling of the photodiodes, circuit design, implementation of an integrated circuit, and subsequent testing. We will also study the potential of compressive learning as an alternative mechanism to conventional frame-based sensing and subsequent inference based on CNNs. Through such learning, the compressive samples generated by a prototype chip that we will design in this subproject will be analysed and classified by an algorithm (e.g., a support vector machine) co-designed with the sensor.

As an application scenario for compressive learning we will work on face recognition, which is of special interest for IoT due to the increasing importance of privacy. We will also study how emerging sensory modalities (event-driven vision, depth sensing, multi-spectral sensing) can be coupled with CNNs to increase the performance of embedded vision systems in key metrics such as consumption and inference accuracy.Finally, combining the results obtained in the other subprojects, we will address the design of an IoT system for a specific application scenario.Specifically, we will design a smart camera trap for remote monitoring of animal species in collaboration with researchers from the Doñana Biological Station.This camera will be able to identify animal behaviour of interest to conservationists in remote locations, so it should incorporate network connectivity and be characterised by high energy autonomy.

LIFELINE

Time-Dependent Variability In Integrated Circuits: Foe (And How To Combat It For The Circular Economy) And Friend (And How To Exploit It For A Disruptive Cybersecurity Solution).

PI: **Rafael Castro / Francisco V. Fernández**

Projects Details::
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovación**
Ref: **TED2021-131240B-I00**
Start date: 01/12/2022 End date: **30/11/2024**
Funding: **138.805,00 €**

Computing performance has been improving year-over-year in a wondrous evolution leading to the rise of a modern digital economy and society that require integrated circuits (ICs) to be more functional and reliable, safer, and more secure. Fields like IoT or Cybersecurity are thus now priorities in many research agendas. But early tremors have been arising that are indicative of larger shifts in how variability, culprit of a reliability loss in ICs, is addressed in the industry: if undealt with, ICs will no longer fulfil those capabilities of safety, security, and reliability.

A crucial challenge in this struggle is the ability to accurately predict the impact of said variability. Considerable past research exists but much more effort is needed to further deepen our understanding of variability and allow for yet more effective solutions to mitigate and handle its impact. Both, emerging markets (like autonomous driving, which necessitates enhanced reliability requirements for electronics to meet strict safety regulations and survive their required operational life) and consumer electronics (where minimizing costs is often a primary concern during design, thus superseding reliability concerns), are impacted as consequence. Moreover, recent developments like the movement towards e-waste reduction or the 2021 European Unions right-to-repair legislation, will require manufacturers to ensure a decade of lifetime and supported repairs, which could put variability at the center of the stage. Finally, variability is essential to an important element in the digital transition: cybersecurity. When area and energy resources are scarce (as with wearable devices), adding security with conventional cryptography approaches is not viable, so lightweight cryptographic solutions have been developed, like those using the concept of Physical Unclonable Function (PUF), a hardware security primitive that exploits the intrinsic variability of CMOS manufacturing (time-zero variability or TZV) to ensure security in communications. However, stochastic effects such as Random Telegraph Noise (RTN) or aging, which introduce a timedependent variability (TDV) component, can seriously compromise not only the reliability of the PUF, but the security of data and communications as well.

The LIFELINE project sets its objectives considering the two sides of variability, foe and friend: foe, where its impact must be mitigated to improve reliability (with benefits like reduced global e-waste), and friend, where it can be exploited for cybersecurity and PUFs. In this latter facet, the project intends to explore a disruptive view: while traditionally TZV has been used as the entropy source to exploit, the project will investigate how to exploit RTN instead, with the benefit that RTN as the entropy source can potentially instill better reliability and immunity to aging to the ICs.

By dealing with variability mitigation (for which the project will develop accurate and stochastic TDV circuit simulation techniques) and exploitation (through new secure and reliable PUF using RTN), LIFELINE can contribute to the Ecological and Digital transitions at the same time: mitigation is perfectly in accord with requirements b) and e) of the environmental objective Transition towards a Circular Economy in the EU Taxonomy Regulation for Ecological Transition; working on exploiting TDV as underlying ingredient of PUFs for cybersecurity will promote the digital transition.

ULTIMATE

Smart mULTI-sensor eMbedded platform for advanced nATurE monitoring.

PI: **Jorge Fernández Berni / Ricardo Carmona Galán**

Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovación**
Ref: **TED2021-131835B-I00**
Start date: 01/12/2022 End date: **30/11/2024**
Funding: **186.530,00 €**

The ongoing sixth mass extinction constitutes a critical threat for the future of human civilization because of the associated degradation of ecosystem services. The proposed actions to bend the curve of mass extinction are heterogeneous and depend on the target ecosystem. In this context, technology plays a crucial role to keep a record of the state of species and ecosystems, identify causes of extinction and degradation, assess the effectiveness of mitigation measures, and monitor the evolution of the environment while collecting data to drive future actions and make informed decisions. Manual (i.e., by humans) off-site analytics of the data collected by sensors has been the standard procedure in the conservation field for many years. As the capabilities of sensors evolved, manual information processing became the major limiting factor for full exploitation of the possibilities technology offered.

To overcome this situation, artificial intelligence (AI), and more specifically its embodiment in the form of deep neural networks (DNNs), is expected to be the most important catalyzer of advances in the next few years. At the moment, cloud-based services are transforming the aforementioned classical paradigm of manual off-site analytics into automatic off-site analytics. However, the bottleneck of conveying all the data to the cloud remains. Ultimately, the objective is automatic on-site analytics, that is, the systems deployed for nature monitoring should be able to sense their environment, process the data locally, and digest information of interest forresearchers, managers, and conservationists. The challenges for the successful realization of these capabilities are remarkable. DNNs, which are todays de-facto standard implementation of AI because of their high accuracy in inference tasks, are computationally heavy and memory-hungry,

not only during training but also when it comes to inferring in real deployments. With the present project, we intend to contribute to the realization of automatic on-site analytics through the design and implementation of a sensing-processing edge platform that will integrate and fusion visual, acoustic, and environmental data for smart nature monitoring at prescribed locations. This platform will be constructed under the principles of low power, low cost, and accurate inference i.e., it must provide specialists with very reliable information for them to make decisions with minimum manual analysis. As a first step, in this 2-year project we will make use of off-theshelf components carefully selected for the targeted platform. As a long-term goal, we aim at designing and integrating specific chips on the basis of the experience acquired with commercial components in order to create a miniaturized system in the line of the long-envisioned concept of smart dust.

VIPS-ID

Verifiable, Private, Distributed and Secure Identification of People and Things.

PI: **Iluminada Baturone**

Projects Details:
Type: **Research projec**t
Funding Body: **Ministerio de Ciencia e Innovación**
Ref: **CPP2022-009796**
Start date: 01/09/2023 End date: **31/08/2025**
Funding: **179.090,00 €**

While biometric data are caused by the human genetic variability of faces, fingerprints, etc., a PUF is a physical construction within a thing that harnesses the variations produced during the thing manufacturing process, so that unique responses are provided to given challenges. In the case of electronic things such as IoT devices, electronic PUFs are considered.
However, many biometric data, such as faces and voices, are public, and, hence, can be used maliciously to carry out impersonation attacks. The rapid spread and impressive achievements of artificial intelligence make it easy to replace an individual by a deepfake. In the case of real-world physical things, besides the already known problem of counterfeit goods, there are also now digital twins, which are their indistinguishable digital counterparts.

Since the problems caused by identity thefts can be very dangerous for people, identity data should be contemplated as private and sensitive (biometric data are already contemplated in data protection regulations of many countries).

The main objectives of the project VIPS-ID will be to provide a verifiable, private, distributed, and secure identification of people and things:

- Identification should be verifiable because there should be external evidences or proofs of the process in order to allow true traceability and auditability.
- Private because intermediate actors should not be able to obtain information about the individual or thing from the external evidences of the identification process.
- Distributed to avoid that a centralized entity could be the unique point of failure or attack.
- Secure by using adequate cryptographic constructions.

These objectives are in line with Spains Recovery and Resilience Plan, mainly to foster Digital Transition. VIPS-ID will increase Cybersecurity in Spain, which is one of the tenth strategic pillars of España Digital 2026. Also, Cybersecurity is one of the three key strategic digital capacities of the Digital Europe programme.
SMARTRANS

SMARTRANS

CMOS-LIDAR: CMOS-SPAD TOF SENSORS FOR FLASH-LIDAR

PI: **Ricardo Carmona Galán / Jorge Fernández Berni**

Projects Details:
Type: **Research project**
Funding Body: **Agencia Estatal de Investigación (AEI)**
Ref: **PDC2022-133933-C31**
Start date: 01/12/2022 End date: **30/11/2024**
Funding: **57.385,00 €**

This proof-of-concept project intends to complete the transference of research results derived from project ENVISAGE: enabling vision technologies for integrated intelligent transportation. In these last three years, despite the difficulties introduced by the global health threats, we have managed to identify some components which we consider critical for the development of intelligent vehicles and transportation infrastructure. These components are intimately related with the awareness of both vehicles and roads, what in the end means the efficient capture and processing of sensory data in severely restricted conditions in terms of computing power, memory and energy resources.

Advances in image sensing technologies and embedded object detection and image recognition have boosted the expectations for the computer vision market: $26.2 billion by 2025, combining hardware, software and services. One of the areas being influenced by the irruption of advanced sensing technologies in combination with embedded intelligence is the development of smart transportation platforms and systems. In the automotive sector, all agents agree that the incorporation of artificial intelligence and the exhaustive exploitation of inter-vehicle and vehicle-to-infrastructure interactions is the most reliable technological route to the autonomous car. Also in UAVs, vision emerges as an essential tool for navigation and autonomous path, and mission planning. During our work in ENVISAGE, we have been able to explore an application scenario, intelligent transportation systems, that is challenging in many aspects:

- Image sensors adapted to these application environments need to operate at high speed, they have to cover a high dynamic range, because they need to deal with diverse lighting conditions, and feature a high sensitivity at low light. And, finally, and this is critical despite not-so-well-founded scepticism, there is a need for cost-effective depth sensing technologies.
- The effective reduction of the visual data flow in favor of distinctive features can be the key to practical implementation of embedded vision systems. The scientific community is focused on developing strategies that efficiently reduce the computational load of deep neural networks (DNNs) while keeping the advantages they have brought about. These strategies cover from the design of the sensor itself [8], to mixed-signal processing schemes, hardware acceleration, or dataflow organization. In the post-Moore era, tailored domain-specific architectures run much better; says David Patterson.
- One critical aspect of the successful deployment of smart transportation infrastructure, and the IoT in general, is power management and energy harvesting. A certain level of autonomy can prevent, for instance, the influence of noisy power lines inside a vehicle. It can also enable the development of always-on traffic-monitoring infrastructure. In these scenarios, energy harvesting permits vision nodes operating exclusively on batteries.

In these three topics, contributions achieved during ENVISAGE have reached a maturity that allows for technology transference and the development of pre-industrial prototypes that will promote successful exploitation as innovative products.

RADIAN

RAdiofrequency/Digital Interfaces managed by Artificial Neural networks.

PI: **José M. De La Rosa**

Projects Details:
Type**: Research project**
Funding Body: **Ministerio de Ciencia e Innovación**
Ref: **PID2022-1380780B-I00**
Start date: 01/09/2023 End date: **31/08/2026**
Funding: **124.375,00 €**

The research carried out in this project will focus on the design of software-defined Radio-Frequency (RF)/digital interfaces assisted by Artificial Neural Networks (ANNs) for energy-aware AIoT devices. These RF/digital interfaces are made up of an Analog-to-Digital Converter (ADC) in the receiver, and a Digital-to-Analog Converter (DAC) in the transmitter. The target is to digitize a wide spectrum of signals with 812-bit resolution within a programmable 30kHz-300MHz bandwidth and a tunable carrier frequency ranging from 0.4GHz to 6GHz. With this objective in mind, a new generation of Sigma-Delta Modulation based RF-to-digital interfaces for AIoT will be developed together with an auxiliary RF Energy Harvesting (RFEH) circuitry. The operation of the circuits will be managed by an ANN to identify energy emitted by nearby wireless devices such as mobile phones and Wi-Fi routers and scavenge RF energy according to the information sensed from the electromagnetic environment. Although the project will cover aspects related to the whole wireless system, it will make emphasis on the design of AI-assisted energy-aware RF ADCs and DACs integrated in nanometer (28nm) CMOS technologies. The project will provide efficient chip solutions in diverse applications dealing with wireless AIoT, while targeting specifications which are at the cutting-edge of the state of the art on analog/digital interfaces. The design of the chips will be supported by an ANN-based design methodology and CAD tools to automate and optimize the design of analog and mixed-signal circuits, and very specially ADCs and DACs.

The project addresses some design challenges towards a more efficient digital transformation directly linked to the strategic actions of the National Program for Scientific & Technical Research, and Innovation (Plan Estatal de Investigación Científica, Técnica y de Innovación, PEICTI 2021-2023), and more specifically with strategic action AE4 Digital World, Industry, Space and Defense. It is also aligned with Goal 9 - Industries, Innovation and Infrastructure of the Sustainable Development Goals (ODS) of the United Nations

SIP-SEXI

Systems in Package for Space Exploration Instrumentation.

PI: **Diego Vázquez**

Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovación**

Ref: **PID2022-137518OB-C22**
Start date: 01/09/2023 End date: **31/08/2026**
Funding: **115.000,00 €**

IMSE/US have a large experience on the development of radiation hardened ASICs and mixed-signal IPs and digital libraries at different CMOS technologies (350nm, 180nm, 65nm), some of them also demonstrated to operate at temperatures as low as -180ºC. Such IPs are qualified and probed in the context of different ASICs previously integrated. Such IPs, and other news to be designed if considered, are intended to be integrated (through Europractice) as bare samples and exploited in the context of the project. This can be understand as a novelty in terms IPs for SiPs ready for extreme low temperature operations. This way, these IPs owned by IMSE/US together with parts accessible in the market can form a library/stock that can be enriched over time.

This project pursues the development of its own SiP capacity, in accordance with the instrumentation and devices planned for its application on Mars within the project (low temperatures, impacts, vibrations, etc.). On the other hand, it also pursues the creation of a stock of integrated IPs (already probed at low temperatures) and comercial circuits as bare dies for its use for SiPs integration. It will allows the creation of SiPs with a drastical reduction of time and associated cost with respect ASIC solutions but taking advange of miniaturization capability and performance improvement with respect a discrete solution. All this work are concentrated in two lines:

- Development of SiP integration capability for the miniaturization of systems and instruments.
- Internal Set of Parts/Bare dies: Identification, integration and characterizaton of a selected set of hardened IPs compatible with low temperatures and identified in the context of the project as of special interest.

TIRELESS

ReliabiliTy, securIty and eneRgy Efficiency in eLectronic dEviceS and circuitS for IoT edge.

PI: **Francisco V. Fernández / Rafael Castro**

Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovación**
Ref: **PID2022-136949OB-C21**
Start date: 01/09/2023 End date: **31/08/2027**
Funding: **203.500,00 €**

The TIRELESS project tackles the variability conundrum in electronic devices and integrated circuits and aims at unraveling the associated challenges of reliability, security and energy efficiency, with one particular electronic system in mind: the internet-of-things (IoT) edge devices. These are powered by nanoelectronic circuits and systems, which exploit nano-CMOS devices and, in the nearby future, beyond- CMOS devices. All these technologies are plagued with a plethora of variability-related phenomena, with multiple aspects in relation to the challenges above. Inadequate handling of the variability impact goes against energy efficiency since guaranteeing certain performances under parametric variations usually implies overdesign including, more often than not, additional energy consumption. Considering variability, at design time and/or during operation, is also essential to extend the lifetime of the integrated circuit and to ensure reliability and safety. Last but not least, some of the variability phenomena can be exploited for lightweight cybersecurity solutions, essential in tiny IoT edge devices.

Accordingly, this project addresses the improvement of the reliability, cybersecurity and energy efficiency of IoT elements by exploiting new solutions for: device characterization and modeling in nano-CMOS and beyond-CMOS technologies, impact evaluation in circuits, circuit design, cryptographic hardware primitives and emerging design paradigms.

From the reliability and energy efficiency point of view, TIRELESS will develop a lab digital twin to elaborate parameter extraction methodologies of time-dependent variability (TDV) in nano-CMOS devices with dramatically enhanced accuracy (as it determines the longterm prediction accuracy) and efficiency (as models must be determined from short experimental time windows). Long-term prediction of circuit performances depend also on the strategies for circuit reliability simulation. To account for this, reliability simulators will be improved to increase their accuracy and account for realistic circuit workloads. Such models and simulation tools will enable circuit synthesis with the best trade-offs between reliability/performances/energy efficiency and the creation of TDV-aware digital libraries enabling reliability-aware digital synthesis. However, in an increasing variability context, reliability-aware synthesis will have to be complemented with on-chip aging monitors that could be used to prevent failures during real-time circuit operation.

The starting point for beyond-CMOS technologies is much more immature. For GFETs and TFTs, Time-Zero Variability (TZV) is predominantly related to the immaturity of the fabrication technology and TDV knowledge is limited. This scenario requires a multiscale characterization approach. The first stage for the reliability-aware design of circuits implemented with these technologies is the introduction of TZV and TDV into compact models for circuit reliability simulation. New computing architectures, such as neuromorphic computing, will also be needed, eventually implemented with memristors.

From the cybersecurity point of view, device variability in nano-CMOS and beyond-CMOS technologies is exploited as a source of entropy for physical unclonable functions for identification and authentication purposes as well as for true random number generation. An additional security-related goal is to exploit variability to fight counterfeiting ICs.

EUPHORIC

Foveated Neuromorphic Sensing and Processing Hardware for Robotic Applications

PI 1: **TERESA SERRANO GOTARREDONDA**

PI 2: **LUIS ALEJANDRO CAMUÑAS MESA**

Projects Details
Type: **Research project**
Funding Body: **Agencia Estatal de Investigación**
Ref: **PID2023-149071NB-C51**
Start date: 01/09/2024 End date: **31/08/2028**
Funding: **184.375,00 €**

EUPHORIC proposes the development of a bioinspired sensing and processing subsytem. During the project, a novel electronically foveated dynamic vision sensor with an on-chip integrated smart digital controller of the foveation regions will be developed. In its normal default mode, the sensor produces a low-resolution output that is processed by a visual attention system which detects the regions of interest in the visual scene that are configured as high resolution in the sensor in real-time. Each of the high-resolution regions of interest will be processed by a small-size recognition system. Thus, the size requirements and power consumption of the recognition system are reduced.

In order to realize the visual feature extraction in the visual recognition system, the project proposes the interconnection of the sensor with a neuromorphic CMOS-memristive processor with on-line learning capability. The neuromorphic processor proposed in the project will be an advanced multicore processor equipped with reconfiguration and programmability capabilities of the different cores which allows the parallelization of the different regions of interest processing. Additionally, in the proposed prototype we will introduce circuit design and algorithmic techniques for analog learning of the memristive synaptic weights. The sensing and processing neuromorphic modules of the EUPHORIC project will be interconnected to audio sensing modules, stochastic processors, and robotic platforms of the other subprojects to develop demonstrator systems of sensing-processing-actuation in high-speed low-power applications.

ELIXIR

Enhancing visuaL perceptIon with neXt-generatIon intelligent infraRed vision sensors

PI 1: **JUAN ANTONIO LEÑERO BARDALLO**

PI 2: **ÁNGEL BENITO RODRÍGUEZ VÁZQUEZ**

Projects Details
Type: **Research project**
Funding Body: **Agencia Estatal de Investigación**
Ref: **PID2023-147244OB-I00**
Start date: 01/09/2024 End date: **31/08/2027**
Funding: **130.000,00 €**

This project targets research of novel event-based sensor architectures for incorporating image analysis structures and hence, visual perception capabilities to InfraRed (IR) imaging defense systems. The rationale for the endeavor is that the incorporation of image analysis capabilities at the edge has been barely explored for IR sensors to date, despite the significant increase in the demand for intelligent IR imaging systems in many application scenarios, including defense as relevant area addressed in this proposal.

Such increased demand has prompted significant development at the sensing edge, including uncooled photonic sensors based on Vapor Phase Deposition (VPD) of materials to implement different types of IR-sensitive diodes, like HgCdTe or PbSe, with enhanced sensing capabilities. The heterogeneous combination of these enhanced sensors with CMOS Focal Plane Arrays (FPA) consisting of the new generation of mature vertical integration technologies defines the conceptual framework for the proposal of new generations of high-speed and low-cost IR vision systems with pixels capable of performing intelligent tasks with small area footprint and competitive pitch.

In parallel, over the past decade, the industrial interest in event-based Dynamic Vision Sensors (DVS) with in-pixel intelligence has experienced unprecedented growth. Esteemed multinational vision sensor developers, including industry giants such as Samsung, Sony, Omnivision, and Prophesee, have swiftly integrated DVS sensors into their comprehensive sensor catalogs. However, implementing DVS sensors in the IR domain is still incipient. Commercial IR image sensors do not perform focal plane processing at the pixel level.

For the given reasons, the actual context is propitious to the development of novel IR vision sensors with

event-based operation and in-pixel processing capabilities. The proposal lies on the previous expertise and trajectory of the proposing group regarding CMOS vision sensor chips with event-based operation for the visible part of the light spectrum, whose achievements include significant academic production, patents, and the transfer to industry.

HIGHLOAWALLET

Crypto-biometric techniques and hardware-enabled solutions for self-sovereign identity wallets with high level of assurance

PI: **ILUMINADA BATURONE CASTILLO**

Projects Details
Type: **Research project**
Funding Body: **Agencia Estatal de Investigación**
Ref: **PID2023-150809OB-I00**
Start date: 01/09/2024 End date: **31/08/2027**
Funding: **184.500,00 €**

In a digital world, electronic transactions require secure digital identities (also known as electronic identities or eID). The legal framework for Spain, as a European country, is the eIDAS (electronic IDentification, Authentication and trust Services) regulation 910/2014. The revision in 2021 of eIDAS established the requirements for the European Digital Identity Wallet (EUDIW). The Commission's aim is that by 2030, 80% of the population within the Union will have this European digital identity and will be able to use it for accessing both private and public services in any Member State. The European scope is to develop wallets that give full control to users on their personal data to share with third parties, and keep track of such sharing, as can be done by Self-Sovereign Identity (SSI) wallets.

The wallet should be univocally associated to its true owner (holder) so that any other people should be unable to hold that identity. This is known as holder binding. Also, the credentials (group of claims about the holder) should be univocally associated to its true wallet, that is, they should not be able to be used by any other wallet owned by other people. This is known as device binding. The project HighLoAwallet will develop SSI wallets with high Level of Assurance (LoA) by using novel crypto-biometric techniques and hardware-enabled solutions that protect these bindings against attacks with high potential, and against duplication and tampering.

The crypto-biometric techniques will ensure verifiability, privacy, and long-term security of multi-modal biometric data associated with the wallet holder. The identity proofing process will verify that the applicant is the physical person identified by the presented multi-modal biometric data, thus ensuring a verifiable physically holder binding. The identification process will be private because intermediate actors should not be able to obtain information about the protected biometric data, which will feature irreversibility, revocability, and unlikability, following the ISO/IEC 24745 standard. The long-term security will be achieved by the use of cryptographic algorithms selected in the NIST Post-Quantum Cryptography Standardization Process.

Since requiring every citizen to own a flagship device with hardware security modules implementing his/her high LoA wallet does not seem realistic, the project HighLoAwallet will employ a remote trusted hardware in the cloud, which is more flexible and cost-effective. The hardware will be identified by the presented responses of Behavioral and Physical Unclonable Functions (BPUFs), thus ensuring a verifiable physically device binding that will avoid counterfeit wallet components and locations outside Europe of personal data. The wallet identification will be private and the BPUF responses will be protected with post-quantum cryptography. The cryptographic and biometric algorithms will be executed in a hardware-enabled secure environment.

Since the wallet will be implemented as a web or hybrid application, the project HighLoAwallet will ensure the remote interactions between holder and wallet (with adequate web authentication), wallet and issuer (with adequate credential issuance), and wallet and verifier (with adequate verifiable presentation). A prototype of SSI wallet with high LoA including the developments achieved in the project will be developed and evaluated in a selected use case.

MEMVIS

Neuromorphic memristive hardware for vision recognition.

PI: **TERESA SERRANO GOTARREDONDA**

Projects Details
Type: **Research project**
Funding Body: **Agencia Estatal de Investigación**
Ref: **PDC2023-145841-C31**
Start date: 01/01/2024 End date: **31/12/2025**
Funding: **115.095,20 €**

The work that will be developed in this proposal is derived directly from the main results obtained in project NanoMem. in NanoMem, a memristive spiking processing chip which was fabricated and tested during that project. In this proposal, we will design a new version of a learning chip for hybrid CMOS-memristors technology based on a 130nm process with OxRAM devices. In this new chip, we will increase the number of neurons and memristors while applying techniques to reduce mismatch between neurons. In parallel, we will develop a demonstrator which will be used to validate the application of the proposed technology in a relevant environment of self-driving cars, increasing the TRL from level 3 achieved during project Nano-mind up to a TRL 5 or 6. This demonstrator will be based on the memristive chip fabricated during Nano-mind (which will be substituted by the new one, eventually), and it will include a new PCB with several compoments (FPGA, microcontroller) which will enable the communication between the memristive chip and a Dynamic Vision Sensor (DVS).

Therefore, the DVS will send events to the PCB in real time, and these events will be processed by the memristive chip with an online learning algorithm so that visual features can be learned in an unsupervised way. Higher-level processing will be implemented in the FPGA and microcontroller, making use of the extracted features to do object recognition. This platform will be applied to the environment of self-driving cars to identify traffic signs in real time.

SARATSO

Asynchronous timing self-optimization for SAR-ADC

PI: **TERESA SERRANO GOTARREDONDA**

Projects Details
Type: **Research project**
Funding Body: **Agencia Estatal de Investigación**
Ref: **PDC2023-145912-I00**
Start date: 01/01/2024 End date: **31/12/2025**
Funding: **73.955,20 €**

This project takes upon the achievements of the StatSET project (RTI2018-098513-B-I00). In the frame of that project, the quality of the test vehicle was not a primary requirement since the objective was to validate a Single-Event simulation flow. However, in order to challenge the simulation flow with high-order effects, we designed an analog-to-digital data converter that is in the state-of-the-art for radiation-hardened parts. In this follow-up project, we want to put the focus on this design and bring the ADC closer to industrialization. The architecture is based on a redundant successive approximation register (SAR-ADC). The redundancy opens the trade-off between resolution and speed because, although it requires some extra comparison cycles, it allows more error budget for settling errors. For an asynchronous implementation, with self-timed successive comparisons, this can be very beneficial.

From an innovation viewpoint, the ASIC has two interesting characteristics: On one hand it implements a self-calibration machine to correct the weights of the feedback DAC that includes a mechanism to account for the comparator offset. This is not trivial in the presence of redundancy. On the other hand, the prototype also implements a tuning mechanism to easily adjust the timing between the successive comparisons. In this follow-up project, we will augment the potential of this tuning mechanism, introducing a low-cost algorithm in the digital section to perform a self-optimization of the asynchronous timing. This will allow the ADC to maximize its performance by adapting to external drifts that may affect the settling properties (aging, temperature, sampling frequency changes, total ionizing dose, etc.).

The existing prototype has already shown promising experimental results: a very good low-frequency effective resolution of 11 effective bits over a 2Vpp input range, up to 30MHz of sampling frequency, and over a large temperature range. In addition, the prototype was submitted to a radiation campaign for Single-Event characterization. The radiation-hardening techniques of the ASIC were found efficient, with a Linear Energy Transfer (LET) threshold over 64.2MeV.cm2.mg-1 for Single-Event Latchup (SEL) and a cross-section of only 0.0138 mm2 for Single-Event Transients (SET) at the output (with a stringent amplitude requirement of only 10 Least-Significant Bits, which correspond to 2.4mV).

In this project, we will extend the electrical characterization to higher frequency input signals and widen the temperature range. We will also test several packaging options to assess the sensitivity of the ASIC to inductive parasitics. In addition, we will complement the SEE radiation data by characterizing the performance drifts associated with the Total Ionizing Dose.

AIR CHIP

Artificial-Intelligence managed Radiofrequency digitizer Chip.

PI: **JOSÉ MANUEL DE LA ROSA UTRERA**

Projects Details
Type: **Research project**
Funding Body: **Agencia Estatal de Investigación**
Ref: **PDC2023-145808-I00**
Start date: 01/01/2024 End date: **31/12/2025**
Funding: **241.879,00 €**

This project aims to design a Radio-Frequency (RF) Analog-to-Digital Converter (ADC) chip managed by Artificial Intelligence (AI) algorithms with application in Software-Defined-Radio (SDR) and Cognitive-Radio (CR) transceivers for 6G mobile terminals and IoT devices. The target is to digitize RF signals with an adaptive 8-to-12-bit effective resolution within a programmable 30kHz-to-300MHz bandwidth, and a tunable carrier fre-

quency ranging from 0.4GHz to 6GHz. The operation of the system will be managed by an embedded Artificial Neural Network (ANN) engine which, based on the information sensed from the electromagnetic spectrum, will predict the least occupied frequency band to establish the communication. A proof-of-concept (POC) chipset demonstrator will be implemented at prototype level in a 28-nm FD-SOI technology provided by ST Microelectronics and an implementation plan will be coordinated with Seamless Waves company (https://seamlesswaves.com), whose Chief Executive Officer (CEO) is one of the external collaborators in this project.

The design of the system will be supported by an ANN-based optimization methodology and it will apply the circuits and systems techniques developed in prior project named CORDION (Cognitive Radio Digitizers for IoT Nodes. Ref. PID2019-103876RB-I00).

The POC chipset developed in this project addresses some design challenges towards a more efficient digital transformation linked to the strategic actions of the National Program for Scientific & Technical Research, and Innovation (Plan Estatal de Investigación Científica, Técnica y de Innovación, PEICTI 2021-2023), and more directly with the strategic action AE4 Digital World, Industry, Space and Defense. Within the framework of the Recovery, Transformation and Resiliency Plan, the present project targets research activities intended towards a digital transition such as the use of disruptive technologies towards an ecological and sustainable transition. It is also aligned with Goal 9 - Industries, Innovation, and Infrastructure of the Sustainable Development Goals (SDG) of the United Nations. The project directly contributes to the Microelectronics and Semiconductors Strategic Plan in Spain, known as PERTE CHIP, which aims to strengthen the design and production capabilities of the Spanish microelectronics and semiconductor industry. In particular, the activity carried out in the project is directly aligned with the following thematic line: (a) Micro/Nanoelectrónica. Diseño, procesos y tecnologías para Circuitos Integrados, and as secondary line (b) RISC V: diseño de procesadores con arquitecturas RISC-V. The POC proposes an innovative way of digitizing RF signals in next-generation 6G mobile terminals and AIoT devices based on a more efficient use of the electromagnetic spectrum with the aid of AI-assisted RF/digital interfaces.

ASIC-IMTER

Proof-of-concept ASIC for thermal impedance measurements in the frequency domain.

PI: **SERVANDO ESPEJO MEANA**

Projects Details
Type: **Research project**
Funding Body: **Agencia Estatal de Investigación**
Ref: **PDC2023-145889-C21**
Start date: 01/01/2024 End date: **31/12/2025**
Funding: **151.492,00 €**

Subproject 1 of the coordinated ASIC-IMTER project, led by the Microelectronics Institute of Seville, a joint center of the University of Seville and the Spanish National Research Council, aims to participate in the definition of the specifications of a mixed-signal ASIC that, using a specific strategy for measuring thermal impedances, will include all the electronics required for a novel two-dimensional air flow sensor; the design of the ASIC, its validation and testing; the integration of the ASIC with the transducers developed in subproject 2 (by the research group in micro and nanotechnologies of the Polytechnic University of Catalonia), in order to constitute a complete sensor system; and the testing and characterization of the complete system in environments close to its final application.
The pursued wind sensor has application in aircraft with adaptive morphology or adaptive aero-elastic wings, which require a network of airflow sensors embedded in the surface of wings and fuselages. The same integrated electronics targeted by the project will serve similar but different application sensors, such as heat flux measurement on the surface of regoliths, also based on thermal impedance measurements.

The methodological and architectural proposal of the ASIC to be designed and tested, is derived from previous results, and results in an efficient implementation in terms of area and power, is robust, and provides accurate thermal impedance results in the frequency domain (magnitude and phase vs. frequency) without the need for numerical post-processing of the acquired data. This makes feasible the miniaturization of sensors, and ultimately, the integration of small sensor networks and providing final results, without the need for high bandwidth data transmissions or specific computational systems.

Both the ASIC and the sensor system as a whole constitute proofs of concept of novel approaches in their respective fields, with multiple applications in a variety of additional fields..

HARD ID WALLET

Proof of concept of hardware security solutions required by the cryptography and biometrics of digital identity wallet.

PI: **ILUMINADA BATURONE CASTILLO**

Projects Details
Type: **Research project**
Funding Body: **Agencia Estatal de Investigación**
Ref: **PDC2023-145873-I00**
Start date: 01/01/2024 End date: **31/12/2025**
Funding: **160.930,00 €**

The ability to establish individual digital identities of natural persons uniquely, accurately, quickly and securely is critical in our hyper connected digital world. The application considered in this project, the digital identity wallet, is the basis of the digital identity (also known as electronic identity or eID).

The identity verification market is forecast to more than double from $7.6 billion in 2020 to $15.8 billion in 2025, a 15.6 percent compound annual growth rate, according to a report from Markets and Markets. In the case of Europe, the European Digital Identity (EUDI) wallets is part of the priority projects identified for the period 2019 - 2024 and is within the goals of the European Digital Agenda 2030. The European Commission's aim is that by 2030, 80% of the population within the Union will have this European digital identity and will be able to use it for accessing online services in any Member State.

To carry out an identification, the user of the wallet typically proves: (a) to know a unique secret (what you know), (b) to have a unique possession (what you have), and (c) to be a physical entity (who you are). The use of two different authentication factors is mandatory in order to reach a substantial Level of Assurance (LoA). For LoA High, the eID solutions must be protected against attacks with high potential, and against duplication and tampering. As specified by ENISA (the European Union Agency for Cybersecurity), a LoA High can be achieved by embedding cryptographic key material in tamper-resistant hardware security module if possession-based authentication factors are used, and ensuring trusted environment if biometric data are used.

There are many platforms, like smartphones, that do not provide direct access to their Trusted Execution Environments (TEEs) but theauthentication technology is proprietary of the platform manufacturer and their hardware solutions are not transparent. Currently, many proposals of EUDI wallets do not provide this high security or provide it by using a technology from outside the EU. The global objective of the Hard-ID-wallet project will be to provide the secure hardware solutions required by the cryptographic and biometric components of digital identity wallets. Hence, it will contribute to the Strategic Project of Microelectronics and Semiconductors, known as PERTE CHIP, in line with the European Chips Act.

Hard-ID-wallet will focus on developing the research results obtained in the project entitled Trusted and post-quantum secure hardware for wallets of decentralized identities using bio and device metrics that need to be transformed into a value creation process, in order to achieve: (1) the incorporation of the results based on Behavioral and Physical Unclonable Functions (BPUFs) and True Random Number Generators (TRNGs) into the secure hardware of the wallet; (2) the inclusion of the results on blockchain non-fungible tokens (NFTs) to allow the wallet to follow a decentralized model of identification; and (3) the inclusion of novel crypto-biometric algorithms to bind the wallet to its user, allowing its verification using a decentralized model with post-quantum security that preserves privacy.

The proof of concept could be very close to a commercial product offering the highly secure cryptographic and biometric wallet components as a service. We estimate that this service could be very interesting for many and diverse wallet users.

DIGISOLAR F2

New Asynchronous Digital Sun Sensor for NewSpace Applications with Event-Based Architecture, Phase 2.

PI: **JUAN ANTONIO LEÑERO**

Projects Details
Type: **Research project**
Funding Body: **Ministerio de Industria y Turismo**
Ref: **AEI-010500-2024-10**
Start date: 12/11/2024 End date: **08/07/2025**
Funding: **54.541,00 €**

The NewSpace revolution has driven the development of new technologies in the space industry, among which the digitalization of the main subsystems that make up a satellite stands out, with the objective of increasing performance, improving interoperability, and reducing costs. In this new paradigm, attitude control systems, responsible for correctly positioning and orienting satellites in orbit, play a fundamental role given the demanding requirements of the new satellite constellations dedicated to providing telecommunications and Earth observation services. The goal for the future is that satellites within these constellations will be able to communicate and accurately position themselves relative to each other, without relying exclusively on control from the ground segment.

DIGISOLAR aims to make unprecedented progress toward full digitalization of the sun sensor, introducing a novel asynchronous data readout technique with an event-based sensor architecture. The objective is to improve on the current technology of sun sensors based on photodiodes and analog interfaces by signifi-

cantly reducing power consumption, simplifying the communications interface by making it digital, achieving total immunity to albedo, and improving accuracy, all while maintaining high robustness against radiation.

DIGISOLAR is therefore part of an industrial research activity and applies to the space segment, for the first time, new technologies related to digitalization and Industry 4.0. It is important to highlight that a digital, albedo-immune, high-performance sun sensor has been one of the ESA's technological objectives for roughly three decades, and that after reviewing the state of the art, no research has thus far been carried out using the sensor architecture proposed in this project.

In this second phase, the DIGISOLAR F2 consortium, with a total budget of €371,847.37, is led by an AEI (Andalucía Aerospace Cluster) and is composed of a public research organization (University of Seville – Institute of Microelectronics of Seville), a large company (Alter Technology), two technology-based SMEs (Solar MEMS Technologies and Simetrycal), a technology-based start-up (FOSSA Systems), and a non-profit cluster association (SECPHO).

DEDOSS

Exploration of dedicated computers for open scientific scenarios.

PI: **ANTONIO JOSÉ ACOSTA JIMÉNEZ**

Projects Details
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovación**
Ref: **RED2022-134244-T**
Duración: **2 años**
Funding: **20.000,00 €**

Computing techniques have advanced very rapidly in recent years. This has made it possible to address new scientific challenges. Calculations that were not manageable a few years ago can now be assumed with a greater probability of success.

This network aims to explore new scientific scenarios and find a way to tackle them with the help of special purpose computers. It will focus on 4 specific fields of action: machine learning for companies and research, spin glasses, hard optimization and quantum computing. All these areas are highly topical, for example the "Quantum Spain" project has recently been launched in Spain to foster the application of this technology among researchers and companies.

This network intends to discuss and increase knowledge both from the point of view of algorithm development and the hardware necessary for its execution. Hardware and software will be studied in parallel to find which combination is best suited to address the different scientific challenges.

The network is solid and compact. Experts in the development of artificial intelligence algorithms, quantum emulation and complex systems will work together with experts in FPGA-type processors, GPU development and ASIC technology. In this way, it will be possible to establish realistic scenarios that are the basis for future studies, funding calls and business applications.
The groups from the University of Zaragoza, the Complutense University of Madrid and the University of Extremadura are close collaborators of Giorgio Parisi, recent Nobel Prize in Physics, they have shared numerous scientific studies with him supported by a large number of publications in high-impact scientific journals and we will try to count on his opinions and participation in webinars and meetings.

During the development of the network, internal debate and learning activities will be organized among its members. External activities will also be carried out to promote the use of advanced technologies in industry and private companies. Each year the members of the network will meet at least twice in person and twice via online. With the aim of working in an open way, on the website created by the network, as well as on social networks, topics of debate, concerns and knowledge arising from the meetings will be shared, which will help promote new projects and foster the entities interest for future calls.

RISC-V

Red-RISCV: Research, Training and Innovation in RISC-V Systems and Open-Source HW/SW.

PI: **PIEDAD BROX JIMÉNEZ**

Projects Details
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovación**
Ref: **RED2022-134618-T**
Duración: **2 años**
Funding: **20.300,00 €**

Currently, there are multiple commercial processors available for HW/SW system development, but all of them are cores with a closed, protected, and proprietary instruction set architecture (ISA), whose use is subject either to costly exploitation licenses or limited to the components and development systems available on the market. One example is the RISC ARM processor family, which currently dominates the market. Any SoC (System on Chip) that includes an ARM core is subject to royalty payments through either purchasing the IP from the core's designer or acquiring an architectural license.

All this is happening at a time when open-source software is already a reality, which has greatly facilitated its evolution, adoption, and adaptation for specific applications. Likewise, in the field of microelectronics and from the perspective of developing specific SoCs, fabrication processes are becoming increasingly accessible and viable both technically and economically—except when a proprietary processor core is included, in which case the license fees and underlying infrastructure costs become prohibitive for most companies.
Over the past decade, an initiative that originated at the University of California, Berkeley has gradually taken shape: the development of the RISC-V processor, an open and public ISA that eliminates most of the restrictions imposed by proprietary ISAs and makes such architectures royalty-free and accessible to any company, paving the way toward open and free hardware.
Just as ARM processors dominate today's market, it can be said that the expansive momentum of the ecosystem created around RISC-V is shaping future trends and strategies, and promises the rapid democratization of hardware and its advance toward open-source HW/SW. In fact, the European Commission has identified the open RISC-V ISA as the ISA of the future European

accelerator within the framework of the European Processor Initiative (EPI). This design is being led by the Barcelona Supercomputing Center (BSC), co-promoter of this network along with the National Center for Microelectronics (CNM).

This proposal places particular emphasis on the necessary combination of two complementary profiles to solidly cover the entire development chain—from the concept at the system level to fully validated chips operating in the final application. In other words, we combine expertise in Microelectronics and in Computer and Systems Architecture, all oriented toward open-source HW/SW.

This is the context in which the present research, training, and innovation network proposal is framed. The network is directed toward these new open architectures in order to ensure that researchers, professors, students, and professionals in this field join in time with this emerging technology, which still lacks a critical mass of qualified personnel, dedicated development infrastructure, and established applications.

The overarching goal of the network is to bring together a critical mass of groups and individuals and to define a roadmap that will project our ecosystem (R&D, education, professionals, and industry) toward a sustainable framework around open ISA RISC-V architectures.

USECHIP

Agreement of Collaboration and Sponsorship among the University of Seville, Alter Technology Tuv Nord, Knowledge Development for Rugged Optical Communications SL, Ontech Security SL, Teledyne Innovaciones Microelectrónicas SLU, and Woodswallow SL for the endowment of the 'USECHIP Microelectronics Chair' at the University of Seville.

PI: **JOSÉ ANTONIO ACOSTA JIMÉNEZ**

Projects Details
Type: **Cátedras Universidad - Empresa**
Funding Body: **Ministerio de Asuntos Económicos y Transformación Digital**
Ref: **TSI-069100-2023-001**
Start date: 12/09/2024 End date: **30/06/2026**
Funding: **20.300,00 €**

REGIONAL PROJECTS

BIOVEO

BIO-inspired nano/cmos hardware object recognition system with E-fOveal Vision.

PI: **Bernabé Linares Barranco**

Projects Details:
Type: **Research Project**
Funding Body: **Junta de Andalucía**
Reference: **ProyExcel_00060**
Start date: 01/12/2022 End date: **31/12/2025**
Funding: **165.600,00 €**

BIOVEO delves into the new paradigm of bio-inspired, neuromorphic machine vision in which video cameras are not used to record image sequences that are then processed image by image. In living beings, retinas do not capture image sequences. Biological retinas encode dynamic visual scenes as streams of nerve impulses that are continuously sent to the brain and processed. The neuromorphic vision paradigm aims to understand and mimic these sensing and processing mechanisms to develop high-speed and/or low-power artificial vision systems for use in very compact autonomic platforms.

In BIOVEO we will focus on investigating spatio-temporal 'multi-resolution' sensing mechanisms to mimic biological foveal vision. In BIOVEO, the aim is to mimic foveation, but starting from artificial retinas of very high physical resolution. It is proposed to implement in these retinas a way of sending information at low resolution, thus saving energy and time for sensing, communication and processing. The global visual scene is processed at low resolution by attention and recognition mechanisms detecting areas of interest. The field of view will be wide and only the areas determined to be of interest will be sampled at high resolution. We call this mechanism 'e-fovea' or 'e-fovea', and it allows to place the fovea in the desired area with less power consumption and more speed than with a motorised system. Moreover, as an additional advantage, the electronic foveal control system allows the implementation of a 'multi-foveal' system. The spectrum of applications of the proposed system is enormous. For example, in autonomous robotic systems or in self-driving vehicles, it would allow the rapid localisation of objects of interest.

RTN SECURE

Exploiting RTN for ageing-resistant hardware security.

PI: **Elisenda Roca**

Projects Details:
Type: **Research Project**
Funding Body: **Junta de Andalucía**
Reference: **ProyExcel_00536**
Start date: 01/12/2022 End date: **31/12/2025**
Funding: **124.568,00 €**

In an increasingly digitized society and economy, security in all kinds of electronic systems has become one of the biggest concerns, especially when resources are scarce (as with "wearable" devices, where there are severe restrictions in area and energy). Responding to this problem with conventional cryptography approaches is not a viable alternative. To avoid this shortcoming, lightweight (i.e., adapted to limited resources) cryptographic solutions have been developed.
Among these are the ones using the concept of "Physical Unclonable Function" (PUF), which typically exploit the intrinsic variability of CMOS manufacturing (time-zero variability or TZV) to have circuits with unique and unpredictable behavior, essential properties in secure cryptographic systems. These circuits usually have low fabrication costs (in area) and low power consumption and can even be implemented with circuitry that is already being used for other purposes. However, effects such as Random Telegraph Noise (RTN) or aging, which introduce a time-dependent variability (TDV) component, can seriously compromise not only the reliability of the PUF itself, but, and as a result, the security of data and communications as well.

It follows that TDV is, from this point of view, a phenomenon that should be palliated. In this Project, however, we intend to explore the completely opposite view: how to exploit the RTN having in mind that this TDV phenomenon, in the same way that TZV does, provides unique and unpredictable behavior to the circuit. Thus, the RTN-SECURE Project will study methods, techniques, and circuits to exploit the RTN for security, both for unique identifier generation and for random number generation. Furthermore, it will also address how to palliate the effect of circuit aging and TZV on these new implementations. Two pillars will sustain this project: (1) an accurate model of the TDV effects and (2) efficient simulation techniques using such model. Both will be developed in RTN-SECURE and both will allow to convincingly address the goal of exploiting RTN for more robust and efficient hardware security primitives.

CSIC PROJECTS

DEEP-MaX-IMSE PHASE 1

Self-assessment and evaluation framework for scientific and social excellence, Phase 1

PI: **TERESA SERRANO GOTARREDONA**

Projects Details
Type: **Research project**
Funding Body: **CSIC**
Reference: **DEEP-MaX-2024_IMSE,CNM**
Start date: 03/05/2024 End date: **31/10/2024**
Funding Phase 1: **20.000,00 €**

The institute will develop a scientific project focused on strengthening research capacities, international scientific leadership, and the scientific, social, and economic impact of the center's research findings. This financial funding is accompanied by the granting of the ASPIRA-MaX Josefa Barba excellence seal for the IMSE-CNM.

I-COOP 2022

Transfer To Cuban Universities Of Advanced Embedded Systems Design Technologies For The Strengthening Of Innovation And Postgraduate Training Capabilities.

PI: **Piedad Brox Jiménez**

Projects Details:
Type: **Research project Funding**
Body: **CSIC**
Reference: **COOPB2022**
Start date: 01/01/2023 End date: **31/12/2024**
Funding: **23.987,40 €**

Continuous advances in microelectronics technologies have led to the development of devices and hardware support that provide an increasing variety of resources for the implementation of digital embedded systems. These include reconfigurable hardware devices (FPGA and SoC-FPGA) and developments based on open hardware (such as RISC-V), which facilitate the realisation of complex digital systems by combining hardware and software elements in an embedded system. The implementation of these systems is essential for the development of the applications and services that underpin today's Digital Society, including those related to the Internet of Things (IoT), which is why they are of wide international relevance.

In tandem with these advances, new development ecosystems have also emerged, including methodologies and design environments that facilitate increased designer productivity and rapid introduction of results, thus boosting the development of innovation projects. These include current development environments for IoT applications; or existing ones for hybrid hardware/software realisations based on reconfigurable hardware and/or open hardware, which allow development processes to be carried out at a high level of abstraction.

On the other hand, the COVID-19 pandemic in the last two years has seriously limited the mobility and direct interaction actions that are fundamental for technology transfer. Simultaneously, the pandemic itself implied the need to strengthen resilience capacities through the development of innovation projects, especially in areas related to health, food production and energy saving, closely related to embedded digital systems.

The main objective of the proposed action is the transfer of advanced technologies for the design and implementation of embedded digital systems, based on reconfigurable hardware and open hardware platforms, to Cuban university professors and researchers to promote their introduction in innovation projects, as well as in master's and doctoral programmes with an electronics profile in different Cuban universities. This will allow a decrease in their technological dependence, as well as an increase in innovation activities that will contribute to the achievement of the Sustainable Development Goals (SDGs).

ELEVATE

Optimization and Strengthening Strategy for the Project Office at the Institute of Microelectronics of Seville

PI: **Mª TERESA SERRANO GOTARREDONA**

Projects Details
Type: **Research project**
Funding Body: **CSIC**
Reference: **REDIN23012**
Start date: 01/01/2024 End date: **31/12/2026**
Funding: **158.377,34 €**

The purpose of the proposed action is to optimize and strengthen the Project Office at the IMSE, with the aim of further promoting participation in international projects and maximizing the outcomes derived from such participation. The action seeks to enhance the efficiency and effectiveness of the Office by providing high-quality advice and consultancy to the Institute's researchers in the formulation and submission of international proposals. Furthermore, it aims to continue increasing the number of European and international projects in which IMSE takes part, by identifying opportunities aligned with the institute's capabilities and priorities. This action also intends to optimize the management of ongoing projects, ensuring their efficient and professional execution..

TECHNOQUANTUM

Hardware-based Technologies to Secure Digital Systems in the Quantum World

PI: **PIEDAD BROX JIMÉNEZ**

Projects Details
Type: **Research project**
Funding Body: **CSIC**
Reference: **ILINK24018**
Start date: 01/01/2025 End date: **31/12/2026**
Funding: **29.951,45 €**

The security of most digital infrastructures relies on public key cryptography (PKC), which enables secure communications between entities without sharing any pre-established secret. The robustness of current PKC techniques is based on the computation complexity of two mathematical problems: the factorization of large numbers and the computation of discrete logarithms, which cannot be solved by current computing systems in a reasonable amount of time. However, quantum computing will be able to solve these problems and hence make vulnerable any digital system based on PKC. Therefore, current cryptographic primitives need to be replaced by an upgraded quantum-resistant cryptography, known as Post-Quantum Cryptography (PQC). Providing such PQC requires a multidisciplinary approach combining the expertise of different research teams working in different areas.

This proposal aims to establish a consortium able to identify solutions and potential limitations in the development of microelectronic and nanophotonic technologies for secure digital systems in the postquantum world. To achieve this goal, the TECHNOQUANTUM project will create an international network of expert research teams specialized in system and communications security, software and hardware engineering, and electronic and photonic design. Through a series of seminars, short stays, and meetings, the participants will exchange ideas and validate hypothesis, consolidating already-established collaborations and creating new ones. This will result in a strategic plan to design research projects together and participate in international competitive calls, with the aim of building resilient digitized cities, communities and services (in line with the Sustainable Development Goals, SDGs) to drive societal and economic growth.

DORAITO

Development AI Techniques for the Design, Optimization, and Autonomous Operation of RF-to-Digital Interfaces in IoT Devices

PI 1: **Gustavo Liñán Cembrano**

PI 2: **José Manuel de la Rosa Utrera**

Projects Details
Type: **Research project**
Funding Body: **CSIC**
Reference: **MMT24-IMSE,CNM-01**
Start date: 20/12/2024 End date: **19/12/2028**
Funding: **192.509,90 €**

The project aims to develop and apply new Artificial Intelligence (AI) techniques and tools in the design and operation of Radio Frequency (RF)-to-Digital interfaces for Software-Defined Radio (SDR) transceivers intended for the Artificial Intelligence of Things (AIoT). The specifications of the RF-to-Digital converter, which constitutes the system's front-end, require digitizing a wide spectrum of signals with a programmable resolution of 8-12 bits across a programmable bandwidth ranging from 30 kHz to 300 MHz, and a carrier frequency shifting between 0.4 GHz and 6 GHz. The system's operation will be managed by an Artificial Neural Network (ANN), which could even be integrated alongside the electronic circuitry of the converter, and which will "learn" to predict the most suitable frequency band to establish communication with a reduced level of interference.

The device will combine Spectrum Sensing (SS) techniques with the capabilities of ANNs to extract patterns and generate short-term predictions (hundreds of milliseconds) regarding occupancy, interference, and noise levels in the available bands, and to make autonomous and adaptive decisions about which band to select. In addition, the microelectronic design itself will be supported by a design methodology based on AI algorithms that we have already begun to outline (https://doi.org/10.1109/TCSII.2023.3323886), and which will be further developed and refined during the course of this project. The objective is to obtain neural networks capable of, starting from very high-level system specifications, first generating valid block-level designs, which will be cross-verified through behavioral simulations, and even proposing transistor-level circuit designs, which will then be validated through electrical simulation. Thanks to additional funding sources available within the group, these developments can be brought into practice through a real system implementation in 28 nm technology.

The research carried out within this project is aligned with the technological areas of "Artificial Intelligence", "Sensing", and "Advanced Data Analytics/Edge Computing" identified in Annex I of the present call, and it addresses several design challenges towards a more efficient digital transformation, in line with the strategic actions of the Spanish National Plan for Scientific and Technical Research and Innovation (PEICTI 2021–2023), and more directly with the strategic action AE4: "Digital World, Industry, Space, and Defense".

MOMENTUM BLB

Micromachining, Additive Manufacturing and Advanced Encapsulation Techniques for Neuromorphic Sensing and Massive High-Performance Computing Ultra-Low Power Edge Systems with CMOS Nanotechnologies

PI: **BERNABÉ LINARES BARRANCO**

Projects Details
Type: **Research project**
Funding Body: **CSIC**
Reference: **MMT24-IMSE,CNM-02**
Start date: 20/11/2024 End date: **19/11/2028**
Funding: **409.486,57 €**

The present Project is enclosed in the research line of Neuromorphic Systems at IMSE (www.imse-cnm.csic.es/neuromorphs). With over 30 years of activity, over 15 EU projects portfolio, two successful spin-offs (www.prophesee.ai, www.graimatterlabs.ai), it develops microchips and edge-computing hardware for bio-inspired event-driven vision sensing, computing, and learning systems. The focus is in the development of vision sensing chips exploiting neuromorphic principles on nanometer-scale CMOS technologies, and low-power Edge-oriented computing chips and systems, including the exploitation of emerging nanotechnology memristive synaptic devices. The research line is highly interdisciplinary, covering from vision sensing, nanoscale memristor based computing and learning hardware, computational neuromorphic algorithms, and applications to high-speed and low-power environments.

On the other hand, IMSE is receiving 9 million € funds to start setting up a new cleanroom facility for advanced encapsulation, micro-printing, and additive manufacturing. The present proposal is intended to combine the neuromorphic microchip design experience with the new cleanroom facilities to enhance and exploit new technological and research capabilities at IMSE, applied to artificial intelligence, sensing, high-efficient edge computing and massive data processing of neuromorphic systems. The specific objectives include:

1. Training on 3D additive manufacturing techniques for neuromorphic vision sensors: microlense design and printing on top of available/new neuromorphic vision sensors, adding new imprinted light/infrerred/microwave sensors or learning-enabling devices connected to an underneath CMOS chip.

2. Training on CMOS neuromorphic nanoscale circuit design technologies, ranging from low-power pico-to-nano ampere analog computing circuits, to fast but power-efficient digital communications.

3. Training on nanotechnology synaptic computing devices, such as HfOx memristors, perovskite memristors, nanopore liquid-ionic-based memristors, for exploitation with combined CMOS integrated circuits for low-power learning neuromorphic computing systems.

4. Training on neuromorphic computational architectures for massive data processing, to devise hardware-friendly neuromorphic energy-efficient computing systems. This training would be purely software-oriented, acquiring knowledge on available AI computational tools.

5. Training on vision sensor chip design for neuromorphic-based vision. These vision sensors are known as "Dynamic Vision Sensors (DVS)". The PI is one of the world-wide pioneers in these sensors, is co-founder of Prophesee, the company commercializing the highest resolution DVS camera in the market, and has 5 patents licensed/co-owned with Prophesee.

INTRAMURAL ECOIMSE-IND

Creation of an IMSE-INDustry ECOsystem for microelectronics in the framework of PERTE-CHIP.

PI: **Mª Teresa Serrano Gotarredona**

Projects Details:
Type: **Research project Funding**
Body**: CSIC**
Reference: **20235E215**
Start date: 01/12/2023 End date: **30/11/2026**
Funding: **193.585,11 €**

The main objectives of this project are:

1. To foster collaboration between IMSE, universities and companies to promote the transfer of knowledge and technology. In the initial activities developed in the framework of PERTE, the fundamental need to create an environment of active collaboration that fosters strategic alliances between academia and industry has been detected.

2. Develop an effective methodology to identify, evaluate and transfer technologies and knowledge from IMSE to industry: IMSE will establish a rigorous process to identify technologies and knowledge with potential applicability to industry and clear mechanisms will be established to carry out the transfer effectively. This will ensure that the knowledge and technology generated at IMSE is translated into practical and applicable solutions in industry.

3. The implementation of PERTE has shown that it is undoubtedly necessary to improve the communication and visibility of IMSE towards the industrial sector, highlighting the achievements and capabilities of the institute for which a comprehensive communication strategy will be developed that will include the promotion of successful research, the dissemination of technological advances and the active participation in regional and international events that raise awareness of IMSE's activities.

4. Enhance IMSE's role as a driver of regional development through knowledge transfer to local and regional companies, which will boost innovation and competitiveness in the region. The creation of a catalogue of companies in the surrounding area where the technology developed at IMSE is potentially transferable is foreseen.

INTRAMURAL SETIT

Design of a Secure Element for the Transition of IoT devices to the quantum era

PI: **PIEDAD BROX JIMÉNEZ**

Projects Details:
Type: **Research project**
Funding Body: **CSIC**
Reference: **202450E086**
Start date: 15/02/2024 End date: **14/02/2026**
Funding: **115.868,04 €**

The SETIT project is focused on exploring solutions to facilitate a secure transition of the Internet of Things (IoT) devices in the quatum era. The IoT paradigm has grown up rapidly in recent years and it is supported by functional and heterogeneous infrastructures that are not prepared to face the future quantum attacks. Defined by a network of embedded devices equipped with sensors, processing units, and internet connectivity, IoT offers unparalleled opportunities for enhancing efficiency and convenience of modern digital societies. Nevertheless, the convergence of IoT and hardware security presents distinct challenges: on the one hand, strong measures to protect sensitive information are needed; whereas on the other hand, some applications impose strict constraints, needing low power usage and compact form factors.

A Secure Element (SE), integrating HW functions into a single design, provides a solution to ease the transition of IoT to PQC. A Secure element is a critical component in ensuring the security of interconnected systems in the IoT frame, whereas it is designed to withstand attacks and protect sensitive data. SE encompasses several cryptography functions such as:

- PQC Encapsulation and Decapsulation: the methods for securely sharing a secret among two or more devices to prevent unauthorized access.
- Key Derivation: the generation of one or more keys from a secret value.
- Key Storage: a secure repository for storing cryptography keys.
- Key Generation: the required algorithms to generate pairs (private and public) of keys used in the context of PQC.
- MAC: the generation of authentication codes for message verifications.In essence, the SE plays a pivotal role in the transition of IoT to PQC while enhancing the speed and security of critical cryptographic primitives, contributing also to the overall performance and efficiency of the IoT systems.

The main objective of the SETIT project is the design and validation in a real IoT environment of a SE. To achieve this main target the following specific objectives are purposed:

1. Design of the main building blocks of the SE.
2. Evaluation of the SE performance on programmable logic devices.
3. Integration of the SE in an IoT environment.
4. Exploration of pathways to transfer the SE to the industrial sector.

INTRAMURAL CONTADOR

Time-to-Digital Converters based on Ring Oscillator Delays

PI: **RICARDO CARMONA GALÁN**

Projects Details:
Type: **Research project**
Funding Body: CSIC
Reference: 202450E095
Start date: 15/02/2024 End date: 14/02/2026
Funding: **9.964,56 €**

The overall objective of this project is to design and validate a compact, low-power time-to-digital converter (TDC) in a submicron CMOS technology, as the central element of a solid-state LiDAR front-end.

The lack of efficient depth-sensing technologies is hindering the large-scale deployment of LiDAR units. Elementary rangefinders operate with a laser pointer and a single detector channel. The light pulses emitted by the laser are reflected by objects encountered along the path and detected by the sensor. The time-of-flight (ToF) of the photons is proportional to the distance between the objects and the light source . An accurate estimation of the ToF enables precise distance determination. By scanning the detector across the field of view, a point cloud is generated, which can be transformed into a dense 3D map of the scene. CMOS technology allows the integration of multiple ranging channels on a single chip, effectively creating a 3D image sensor. In doing so, the mechanically aligned and synchronized scanning of emitter and receiver—prohibitively costly—is replaced by software calibration. This is the operating principle of solid-state LiDAR .

Direct ToF estimation using CMOS requires:

- a light-sensitive, CMOS-compatible detector, e.g., a single-photon avalanche diode (SPAD) or an avalanche photodiode (APD) , equipped with adequate avalanche quenching, signal conditioning, and pulse-shaping circuitry;
- and a precise time-interval discriminating circuit, such as a TDC , to register the timing of photon arrivals and the avalanche onset in SPADs, or alternatively, abrupt changes in the photocurrent generated in APDs. In some cases, TDC outputs require filtering to discard irrelevant or spurious measurements.

An important aspect of the TDC to be designed in this project is its ability to be integrated into a sensor chip. This imposes requirements of low power consumption, moderate area footprint, and uniformity guaranteed not only through design but also via additional compensation measures.

Under these constraints, we have worked on a specific architecture that fulfills these requirements, providing a time resolution below the gate delay. This architecture relies on a delay-ring-oscillator-based TDC, which operates as a time interpolator. In this topology, conversion is carried out in two steps: a coarse detection stage, implemented via a counter enabled by the voltage-controlled ring oscillator (VCRO), running at a frequency lower than that corresponding to the target time resolution; and a fine detection stage, carried out by a thermometer-to-binary encoder fed by the internal phases of the VCRO. To generate an even number of phases for the decoder, both true ring oscillators and pseudo-differential oscillators are the most suitable approaches. As for oscillation frequency control, this can be achieved through current-control techniques or by tuning the time constant of the delay cell output.

This class of TDC is the most suitable for per-pixel or per-column implementations , thanks to its reduced area occupation and low power consumption.

AYUDAS INCORPORACIÓN CIENTÍFICOS TITULARES 2024

Extraordinary Grants for the Recruitment of Tenured Scientists corresponding to the 2020-2021 Public Employment Offers

AYUDA 1: **JUAN NÚÑEZ MARTÍNEZ**

Funding Body: **CSIC**
Reference: **2024ICT056**
Start date: 28/06/2024 End date: **30/05/2025**
Funding: **5.000 €**

AYUDA 2: LUIS ALEJANDRO CAMUÑAS MESA
Funding Body: **CSIC**
Reference: **2024ICT057**
Start date: 28/06/2024 End date: **30/05/2025**
Funding: **5.000 €**

AYUDAS IMOVE

iMOVE 2024 Grants for Short Stays in R+D+I Centers or Companies Abroad for PhD Researchers Conducting their Doctoral Thesis at CSIC

AYUDA 1: **ROBERTO MÉNDEZ**

PI: **BERNABÉ LINARES BARRANCO**

Funding Body: **CSIC**
Reference: **IMOVE24061**
Start date: 01/08/2024 End date: **31/07/2025**
Funding: **3.150 €**

AYUDA 2: APURBA KARMAKAR

PI: **PIEDAD BROX JIMÉNEZ**

Funding Body: **CSIC**
Reference: **IMOVE24128**
Start date: 01/08/2024 End date: **31/07/2025**
Funding: **1.240 €**

INTERNATIONAL AND OTHER TYPES OF PROJECTS

Mem2CNN

Hardware realization of universal memory-based memristive cellular computer structures

PI: **Ricardo Carmona Galán**

Projects Details:
Type: **Research project**
Funding Body: **Deutsche Forschungsgemeinschaft (Germany)**
Reference: **441957207**
Start date: 01/06/2024 End date: **31/05/2027**
Funding: **206.450,00 €**

The second phase of project Mem2CNN, is intended to expand the involvement of memristor devices and their unique properties into memristor-based cellular nonlinear networks (M-CNNs). We will explore and implement a novel hardware system that will materialize the M-CNN Universal Machine (M-CNNUM). In the proposed system, memristor devices arranged in a crossbar array configuration will be utilized to implement a family of M-CNN genes.

According to the CNN theory, they can be understood as collections of CNN templates executed in a sequential manner to carry out diverse computational tasks, akin to the algorithmic operations observed in traditional computer systems.

Memristor crossbar arrays can be utilized also as dot-product engines, implementing the necessary multiply-and-accumulate operations for the calculation of offset current. Then, we envisage to combine this novel memristor-based hardware realization with the rich dynamics of the M-CNN core, which offers both local nonvolatile storage and memcomputing capabilities.

HEART-FAIL

Technology transfer and exploitation activities of the device for a heart failure patient monitoring, protected by patent P202131041

PI: **ALBERTO DEL OLMO FERNANDEZ**

Projects Details:
Type: **Research project**
Funding Body: **Fundacion La Caixa**
Ref: **CI22-00287**
Start date: 22/12/2022 End date: **22/12/2024**
Funding: **70.000,00 €**

This project aims to build a wearable medical device and platform to predict early clinical outcomes in patients with acute heart failure. The wearable device will be able to carry out real-time bioimpedance measurements in the patients' legs. The data platform will analyze the patients monitored data to provide the physician a truly personalised decision support system, preventing complications in the treatment of patients.

CONTRACTS

REMOTE MONITORING FOR BIRD SPECIES IDENTIFICATION IN SEO/BIRDLIFE MONITORING PROGRAMS

PI: **JORGE FERNÁNDEZ BERNI**

FUNDING ENTITY: **SEO/BIRDLIFE**

Projects Details:
Type: **TECHNOLOGICAL SUPPORT CONTRACT**
Body: **FIUS**
Start date: 01/11/2023 End date: **31/10/2024**
Funding: **1.900,00 €**

The purpose of this contract is the execution of the project entitled REMOTE MONITORING FOR BIRD SPECIES IDENTIFICATION IN SEO/BIRDLIFE MONITORING PROGRAMS

TECHNICAL CONSULTING FOR THE DEVELOPMENT OF INTEGRATED CIRCUITS OF EMBEDDED SYSTEMS IN THE FIELD OF SECURITY

PI: **PIEDAD BROX JIMÉNEZ**

Projects Details:
Type: **TECHNOLOGICAL SUPPORT CONTRACT**
Body: **CSIC**
Start date: 08/11/2023 End date: **07/01/2024**
Funding: **14.850,00 €**

The purpose of this contract is the execution of the project entitled TECHNICAL CONSULTING FOR THE DEVELOPMENT OF INTEGRATED CIRCUITS OF EMBEDDED SYSTEMS IN THE FIELD OF SECURITY

DEVELOPMENT AND PREPARATION OF CYBERSECURITY VERIFICATION METHODOLOGIES IN INTEGRATED CIRCUITS (SOC AND SIP)

PI: **ERICA TENA SÁNCHEZ**

FUNDING ENTITY: **DEKRA TESTING AND CERTIFICATION S.A.U.**

Projects Details:
Type: **I + D CONTRACT**
Body: **FIUS**
Start date: 01/01/2024 End date: **30/09/2025**
Funding: **120.000,00 €**

The purpose of this contract is the execution of the project entitled DEVELOPMENT AND PREPARATION OF CYBERSECURITY VERIFICATION METHODOLOGIES IN INTEGRATED CIRCUITS (SOC AND SIP) [RISCCOM]

DESIGN AND DEVELOPMENT OF FIRMWARE FOR SMART IMAGE CAPTURE DEVICES

PI: **PABLO PEREZ GARCÍA**

FUNDING ENTITY: **PHOTOBOOTH SUPPLY Co.**
Projects Details:
Type: **TECHNOLOGICAL SUPPORT CONTRACT**
Body: **FIDETIA**
Start date: 29/03/2024 End date: **01/04/2025**
Funding: **39.738,18 €**

The purpose of this contract is the execution of the project entitled DESIGN AND DEVELOPMENT OF FIRMWARE FOR SMART IMAGE CAPTURE DEVICES

STUDY ON THE AUTOMATIC IDENTIFICATION OF BIRD SPECIES IN SEO/BIRDLIFE MONITORING PROGRAMS

PI: **JORGE FERNÁNDEZ BERNI**

FUNDING ENTITY: **SEO/BIRDLIFE**
Projects Details:
Type: **TECHNOLOGICAL SUPPORT CONTRACT**
Body: **FIUS**
Start date: 03/11/2024 End date: **02/10/2025**
Funding: **3.250,00 €**

The purpose of this contract is the execution of the project entitled STUDY ON THE AUTOMATIC IDENTIFICATION OF BIRD SPECIES IN SEO/BIRDLIFE MONITORING PROGRAMS, composed of the following tasks:

- Hardware programming for field recording. Configuration and optimization for audio capture according to the required sampling needs.
- AI analysis. Implementation of advanced analysis using Artificial Intelligence for the interpretation of recordings, providing the identification of the bird species present.
- Platform for visualization, analysis, and efficient management of the collected data.

DESIGN OF INNOVATIVE CHIPS FOR THE FIRST HIGH-PERFORMANCE, LOW-

POWER MULTIFUNCTIONAL INTEGRATED BOARD IN STRATOSPHERIC BALLOONS (CHIP-NESE)

PI: **JUAN ANTONIO LEÑERO**

FUNDING ENTITY: **SOLAR MEMS TECHNOLOGIES S.L.**
Projects Details:
Type: **I + D CONTRACT**
Body: **FIUS**
Start date: 03/06/2024 End date: **01/05/2026**
Funding: **59.400,00 €**

The purpose of this contract is the execution of the project entitled DESIGN OF INNOVATIVE CHIPS FOR THE FIRST HIGH-PERFORMANCE, LOW-POWER MULTIFUNCTIONAL INTEGRATED BOARD IN STRATOSPHERIC BALLOONS (CHIP-NESE)

MINIATURIZED SENSOR FOR LONG TERM MONITORING OF ATOMIC OXYGEN DEGRADATION PROCESSES IN VLEO MISSIONS

PI: **JOAQUÍN CEBALLOS CÁCERES**

FUNDING ENTITY: **INSTITUTO DE ESTUDIOS ESPACIALES DE CATALUÑA (IEEC)**
Projects Details:
Type: **TECHNOLOGICAL SUPPORT CONTRACT**
Body: **CSIC**
Start date: 20/05/2024 End date: **19/11/2025**
Funding: **15.000,00 €**

The purpose of this contract is the execution of the project entitled MINIATURIZED SENSOR FOR LONG TERM MONITORING OF ATOMIC OXYGEN DEGRADATION PROCESSES IN VLEO MISSIONS, subcontract of the contract between ESA and IEEC with No. 4000144432/24/NL/GLC/ov.

SUPPORT FOR THE STUDY OF THE APPLICATION OF PULSED LASER TECHNIQUE FOR SCREENING AND CHARACTERIZATION OF ELECTRONIC COMPONENTS FOR SPACE APPLICATIONS

PI: **JOAQUÍN CEBALLOS CÁCERES**

FUNDING ENTITY: **ALTER TECHNOLOGY TÜV NORD SAU**
Projects Details:
Type: **TECHNOLOGICAL SUPPORT CONTRACT**
Body: **CSIC**
Start date: 03/06/2024 End date: **02/09/2024**
Funding: **1.450,00 €**

The purpose of this contract is the execution of the project entitled SUPPORT FOR THE STUDY OF THE APPLICATION OF PULSED LASER TECHNIQUE FOR SCREENING AND CHARACTERIZATION OF ELECTRONIC COMPONENTS FOR SPACE APPLICATIONS

RESEARCH ON SIMSIDES BLOCKSET

PI: **JOSE MANUEL DE LA ROSA**

FUNDING ENTITY: **THE MATH WORKS INC**
Projects Details Type: **DONATION**
Body: **FIUS**
Start date: 20/06/2024 End date: **19/09/2028**
Funding: **147.200,00 €**

The purpose of this contract is the execution of the project entitled SIMSIDES BLOCKSET

DESIGN OF RECONFIGURABLE MICROELECTRONIC CIRCUITS

PI: **JOAQUÍN CEBALLOS CÁCERES**

FUNDING ENTITY: **UNIVERSIDAD DE GRANADA**
Projects Details:
Type: **TECHNOLOGICAL SUPPORT CONTRACT**
Body: **CSIC**
Start date: 01/10/2024 End date: **15/11/2024**
Funding: **24.000,00 €**

The purpose of this contract is the execution of the project entitled DESIGN OF RECONFIGURABLE MICROELECTRONIC CIRCUITS

CONTRACT FOR TECHNICAL CONSULTING FOR THE DEVELOPMENT OF INTEGRATED CIRCUITS FOR SECURITY APPLICATIONS

PI: **PIEDAD BROX JIMÉNEZ**

FUNDING ENTITY: —-
Projects Details:
Type: **TECHNOLOGICAL SUPPORT CONTRACT**
Body: **CSIC**
Start date: 25/07/2024 End date: **27/12/2024**
Funding: **82.644,63 €**

The purpose of this contract is the execution of the project entitled CONTRACT FOR TECHNICAL CONSULTING FOR THE DEVELOPMENT OF INTEGRATED CIRCUITS FOR SECURITY APPLICATIONS

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  Reviews in Cardiovascular Medicine, vol. 25, no. 9, article 320, 2024
  IMR Press ISSN: 1530-6550

- **Wearable Devices Based on Bioimpedance Test in Heart Failure: Clinical Relevance: Systematic Review**
  Giménez-Miranda, Luis; Scagliusi, Santiago F.; Pérez-García, Pablo; Olmo-Fernández, Alberto; Huertas, Gloria; Yúfera, Alberto; Medrano, Francisco J.
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CONFERENCE PAPERS

- **Positive Neuroblastoma differentiation with AC electrical-stimulation**
  Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society, EMBS
  Martín, D.; Scagliusi, S.F.; Pérez, P.; Olmo, A.; Algarin, A.; Yúfera, A.; Huertas, G.; Daza, P.

- **Exploring Vein Biometrics on Ordinary Smartphones Using CNNs and Transfer Learning with Open and Closed Sets**
  BIOSIG 2024 - Proceedings of the 23rd International Conference of the Biometrics Special Interest Group
  Lopez-Gonzalez, Paula; Arjona, Rosario; Baturone, Iluminada

- **Combining CRYSTALS-Kyber Homomorphic Encryption with Garbled Circuits for Biometric Authentication**
  BIOSIG 2024 - Proceedings of the 23rd International Conference of the Biometrics Special Interest Group
  Arjona, Rosario; Franco, Claudia; Roman, Roberto; Baturone, Iluminada

- **Deep Learning-Based Architecture for RF Frame Detection for CR Applications Using Spectrograms**
  Midwest Symposium on Circuits and Systems
  Rojas, A.; Linan-Cembrano, G.; Dolecek, G. Jovanovic; De La Rosa, J.M.

- **An Educational Innovation Project Focused on the Implementation of Biometrics in Portable Devices**
  16th Congreso de Tecnologia, Aprendizaje y Enseñanza de la Electronica, TAEE 2024
  Arjona, Rosario; López-González, Paula; Arcenegui, Javier; Baturone, Iluminada

- **Design and Modeling of a Plethysmographic Wearable Sensor for Heart Failure Non-Invasive Edema Monitoring**
  2024 IEEE BioSensors Conference, BioSensors 2024
  Maurencig, S.; Palmero, M.; Algarin, A.; Scagliusi, S.F.; Perez, P.; Martin, D.; Huertas, G.; Yufera, A.

- **On the Use of Open-Source EDA Tools for Teaching and Learning Microelectronics**
  16th Congreso de Tecnologia, Aprendizaje y Enseñanza de la Electronica, TAEE 2024
  Galán-Benítez, Ismael; Carmona-Galán, Ricardo; De La Rosa, José M.

- **Coverage Analysis of an RFID System for the Identification and Localization of a Queen Bee in a Hive**
  IEEE Antennas and Propagation Society, AP-S International Symposium (Digest)
  López, José Lorenzo; Llácer, Leandro Juan; Caballero, Javier Fernández; Beltrán, Laura Pérez; Fabres, Marta Cabedo; Bataller, Miguel Ferrando; Restituto, Manuel Delgado

- **Optimization-based bit selection technique to improve the reliability of PUFs**
  Proceedings - 2024 20th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design, SMACD 2024
  De Los Santos-Prieto, F.; Rubio-Barbero, F.J.; Castro-Lopez, R.; Roca, E.; Fernandez, F.V.

- **Streamlined design methodology for Cell-Based DCOs**
  Proceedings - 2024 20th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design, SMACD 2024
  Santana-Andreo, A.; Gata-Romero, J.M.; Castro-Lopez, R.; Roca, E.; Fernandez, F.V.

- **Hardware implementations, SCA/FIA attacks, and countermeasures for the ASCON AEAD cipher: A review**
  2024 39th Conference on Design of Circuits and Integrated Systems, DCIS 2024
  Martin-Gonzalez, Miguel; Tena-Sanchez, Erica; Ordonez, F. Eugenio Potestad; Acosta, Antonio J.

- **Increasing the Accuracy of Spectrogram-based Spectrum Sensing Trained by a Deep Learning Network Using a Resnet-18 Model**
  2024 39th Conference on Design of Circuits and Integrated Systems, DCIS 2024
  Rojas, A.; Dolecek, G. Jovanovic; De La Rosa, J.M.; Linan-Cembrano, G.

- **AISAD: A User-Friedly AI-Assisted MATLAB Tool for the High-Level Design of ΣΔ Modulators**
  2024 39th Conference on Design of Circuits and Integrated Systems, DCIS 2024
  Manrique-Merchan, P.; Linan-Cembrano, G.; De La Rosa, J.M.

- **Harvesting RTN for True Random Number Generators and Physical Unclonable Functions**
  Proceedings - 2024 20th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design, SMACD

2024
Rubio-Barbero, F.J.; De Los Santos-Prieto, F.; Castro-Lopez, R.; Roca, E.; Fernandez, F.V.

- **A novel 10T SRAM bit-cell with high static noise margin and low power consumption for binary In-Memory Computing**
  2024 IEEE 14th Annual Computing and Communication Workshop and Conference, CCWC 2024
  Khosravi, Hossein; Galan, Ricardo Carmona; Fernandez-Berni, Jorge; Kandalaft, Nabeeh

- **Compact 868 MHz RFID-Based Antenna for Queen Bee Identification and Location inside Hives**
  18th European Conference on Antennas and Propagation, EuCAP 2024
  Beltrán, Laura Pérez; López, José Lorenzo; Caballero, Javier Fernández; Fabres, Marta Cabedo; Bataller, Miguel Ferrando; Juan-Llácer, Leandro; Delgado-Restituto, Manuel

- **Electromagnetic Fault Injection Attack Methodology against AES Hardware Implementation**
  2024 39th Conference on Design of Circuits and Integrated Systems, DCIS 2024
  Casado-Galan, A.; Potestad-Ordonez, F.E.; Acosta, A.J.; Tena-Sanchez, E.

- **Towards a Digital Twin of a Time-Dependent Variability Characterization Laboratory**
  Proceedings - 2024 20th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design, SMACD 2024
  Gata-Romero, J.M.; Roca, E.; Castro-Lopez, R.; Fernandez, F.V.

- **A Verilog-A/MS Compact Model for the Temperature Dependency of the Open-Circuit Voltage for Integrated Diodes**
  Proceedings - 2024 20th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design, SMACD 2024
  Fernández-Peramo, Pablo; Leñero-Bardallo, Juan A.; Palomeque-Mangut, Sergio; Rodríguez-Vázquez, Ángel

- **Analysis and Simulation of Reset Leakage Currents and Quantization Error in a PFM Digital Pixel**
  Proceedings - 2024 20th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design, SMACD 2024
  Palomeque-Mangut, Sergio; Fernández-Peramo, Pablo; Leñero-Bardallo, Juan A.; Rodríguez-Vázquez, Ángle

- **Applying Hodgkin-Huxley Neuron Model for Perovskite Memristor in Circuit Simulation**
  2024 IEEE International Conference on Metrology for eXtended Reality, Artificial Intelligence and Neural Engineering, MetroXRAINE 2024 - Proceedings
  Shooshtari, Mostafa; Través, Manuel Jiménez; Pahlavan, Saeideh; Serrano-Gotarredona, Teresa; Linares-Barranco, Bernabé

- **Design and Evaluation of Combined Hardware FIA and SCA Countermeasures for AES Cipher**
  Proceedings - 2024 27th Euromicro Conference on Digital System Design, DSD 2024
  Potestad-Ordonez, F.E.; Tena-Sanchez, E.; Zuniga-Gonzalez, V.; Acosta, A.J.

- **A Discrete Approach to Dynamic Vision with Single-Photon Detectors**
  Proceedings - IEEE International Symposium on Circuits and Systems
  Gomez-Merchan, R.; Leñero-Bardallo, J.A.; Fernández-Peramo, P.; Rodríguez-Vázquez, Á.

- **Integrated Electrode-Based Systems for Stem-Cell Stimulation**
  2024 39th Conference on Design of Circuits and Integrated Systems, DCIS 2024
  Algarin, A.; Martin, D.; Daza, P.; Huertas, G.; Yufera, A.

- **Implementation of a Multiclass Support Vector Machine on a Differential Memristor Crossbar**
  Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems
  Khan, Amir; Ntinas, Vasileios; Fernandez-Berni, Jorge; Carmona-Galan, Ricardo; Tetzlafft, Ronald

- **VLSI integration of a RO-based PUF into a 65 nm technology**
  2024 IEEE Nordic Circuits and Systems Conference, NORCAS 2024 - Proceedings
  Ortega-Castro, Pau; Rojas-Munoz, Felipe; Mora-Gutierrez, Jose M.; Brox, Piedad; Martinez-Rodriguez, Macarena C.

- **Enhancing Dynamic Vision Sensors Performance with a Photovoltaic Receptor**
  Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems
  Fernandez-Peramo, Pablo; Lenero-Bardallo, Juan A.; Rodriguez-Vazquez, Angel

- **Full Open-Source Implementation of an Academic RISC-V on FPGA**
  16th Congreso de Tecnologia, Aprendizaje y Enseñanza de la Electronica, TAEE 2024
  Navarro-Torrero, Pablo; Martínez-Rodríguez, Macarena C.; Barriga-Barros, Ángel; Brox, Piedad

- **Single-Ended to Differential Fully-Integrated LNA for Low Voltage Supply Applications**
  Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems
  Mendez-Romero, Roberto; Peralias, Eduardo; Serrano-Gotarredona, Teresa; Linares-Barranco, Bernabe; Fiorelli, Rafaella

- **Digital Design Flow Based on Open Tools for Programmable Logic Devices**
  16th Congreso de Tecnologia, Aprendizaje y Enseñanza de la Electronica, TAEE 2024
  Navarro-Torrero, Pablo; Rojas-Muñoz, Luis Felipe; Martínez-Rodríguez, Macarena C.; Barriga-Barros, Ángel; Jiménez-Fernández, Carlos J.; Brox, María; Brox, Piedad

- **Mismatch calibration strategy for query-driven AER read-out in a memristor-CMOS neuromorphic chip**
  Proceedings - IEEE International Symposium on Circuits and Systems
  Camuñas-Mesa, Luis; Serrano-Gotarredona, Teresa; Linares-Barranco, Bernabé

- **Project-based learning of digital design: Using RGB LEDs**
  16th Congreso de Tecnologia, Aprendizaje y Enseñanza de la Electronica, TAEE 2024
  Jiménez-Fernández, Carlos Jesús; Oliva, Carmen Baena; Fernández, Pilar Parra; Barrero, Manuel Valencia

- **Live Demonstration: Automated Design of Analog and Mixed-Signal Circuits Using Neural Networks**
  Proceedings - IEEE International Symposium on Circuits and Systems
  Liñán-Cembrano, Gustavo; De La Rosa, José M.

- **When Barkhausen's Criterion Does Not Suffice and you Must Rely on the Forgotten Art of Oscillator Design**
  16th Congreso de Tecnologia, Aprendizaje y Enseñanza de la Electronica, TAEE 2024
  Rodríguez-Vázquez, Ángel; Leñero-Bardallo, Juan A.

- **Design of a Karatsuba Multiplier to Accelerate Digital Signature Schemes on Embedded Systems**
  2024 IEEE Nordic Circuits and Systems Conference, NORCAS 2024 - Proceedings
  Navarro-Torrero, Pablo; Camacho-Ruiz, Eros; Martinez-Rodriguez, Macarena C.; Brox, Piedad

- **Design Lab-Based Learning of Analog Front-End Circuits: A Sigma-Delta Modulator Lab**
  16th Congreso de Tecnologia, Aprendizaje y Enseñanza de la Electronica, TAEE 2024
  Rodríguez-Vázquez, A.; Leñero-Bardallo, J.A.; Gómez-Merchán, R.; Méndez-Romero, R.J.

- **A 1.7-mW 26.5-GHz LC-DCO with Optimum-Q Varactors for 25-Gb/s Automotive Optical Links**
  Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems
  Jimenez-Fernandez, Pablo; Rodriguez-Perez, Alberto; Prefasi, Enrique; Sierra, Francisco; Guerra, Oscar; Del Rio, Rocio

- **Co-optimized training of models with synaptic delays for digital neuromorphic accelerators**
  Proceedings - IEEE International Symposium on Circuits and Systems
  Patiño-Saucedo, Alberto; Meijer, Roy; Detteter, Paul; Yousefzadeh, Amirreza; Garrido-Regife, Laura; Linares-Barranco, Bernabé; Sifalakis, Manolis

- **Live Demonstration: Using ANNs to Predict the Evolution of Spectrum Occupancy**
  Proceedings - IEEE International Symposium on Circuits and Systems
  Liñán-Cembrano, Gustavo; De La Rosa, José M.

- **Dynamic Slope Detection: A High-Compression Fidelity-Preserving Approach for ECG Signal Acquisition**
  Midwest Symposium on Circuits and Systems
  Saenz-Noval, Jorge J.; Lenero-Bardallo, Juan
  Antonio; Gontard, Lionel C.; Tang, Wei

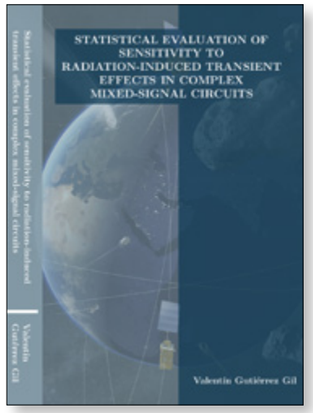
- **Neuromorphic Technology Insights in Spain**
  Proceedings of the IEEE Conference on Nanotechnology
  Iturbe, Xabier; Camuñas-Mesa, Luis; Linares-Barranco, Bernabé; Serrano-Gotarredona, Teresa; González, Mireia B.; Campabadal, Francesca; Margarit-Taulé, Josep Maria; Serra-Graells, Francisco; Terés, Lluís; Lanillos, Pablo; Lopez, Víctor; Bisquert, Juan; Guerrero, Antonio; López-Vallejo, Marisa; Ituero, Pablo; Juarez, Eduardo; Otero, Andrés; Holgado, Miguel; Rubio, Antonio; Rodríguez, Rosa; Picos, Rodrigo; Miranda, Enrique; Suñé, Jordi; Sort, Jordi; Roldan, Juan B.; Jiménez, Francisco; Dueñas, Salvador; Castán, Helena; Cirera, Albert; Marsal, Lluís; Basterretxea, Koldo; Astarloa, Armando; Barranco, Francisco; Linares-Barranco, Alejandro; Jiménez, Ángel; Ollero, Anibal; Martinez-De-Dios, J.R.; Goma, Rafael; Rodrigues, Serafim; Ser, Javier Del; Torres, Elías; Espasa, Roger; Bofill-Petit, Adrià; Turchetta, Renato; Goossens, Stijn; Vergara, Germán; Jonuzi, Tigers; Artundo, Iñigo; Sainz, Unai; Ruiz, David; Gonzalez-Arjona, David; Regada, Raúl; Pedró, Marta; Aramburu, Ander; Lara-Rapp, Oscar; Pérez de Arrilucea, Javier; Terreri, Sarah; Fernández, Marta; Ulloa, Michel I.; Gabarrón, Alfonso

THESIS

Design of a hardware Root-of-Trust on embedded systems

Eros Camacho Ruiz

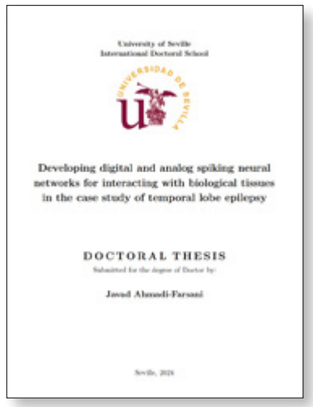
Date of defense: 13/03/2024
UNIVERSIDAD DE SEVILLA, IMSE-CNM



Statistical evaluation of sensitivity to radiation-induced transient effects in complex mixed-signal circuits

Valentín Gutiérrez Gil

Date of defense: 08/05/2024
UNIVERSIDAD DE SEVILLA, IMSE-CNM



Developing digital and analog spiking neural networks for interacting with biological tissues in the case study of temporal lobe epilepsy

Javad Ahmadifarsani

Date of defense: 15/10/2024
UNIVERSIDAD DE SEVILLA, IMSE-CNM

Rad-Hard Design Techniques for High Speed and High Resolution SAR ADCs

Carlos Domínguez Matas

Date of defense: 05/07/2024
UNIVERSIDAD DE SEVILLA, IMSE-CNM

Event-Driven Single-Photon Detectors and Sensors for ToF LiDAR Systems

Rubén Gómez Merchán

Date of defense: 11/07/2024
UNIVERSIDAD DE SEVILLA, IMSE-CNM

TECHNOLOGICAL TRANSFER

Technology transfer is managed at the Seville Microelectronics Institute by the Projects and Transfer Unit (UPT-IMSE). The UPT's fundamental mission is to promote, channel and manage the ideas and outputs resulting from the research staff's projects into innovations at the service of civil society, the public sector and companies. All our research has the ultimate goal of contributing to generating greater social well-being. For this reason, permanent contact and work with the different economic and social agents is a key pillar in the transversal research carried out at the IMSE. The main objectives of the IMSE Projects and Transfer Unit are:

- Identify and protect the research results and innovative ideas developed by IMSE research staff.
- Increase the applicability of investigations by generating permanent contact with interested agents.
- Establish new technology-based companies that allow the development of the technology that arises.
- Commercialize and internationalize research in coordination with the CSIC and the University of Seville.
- Advise the research staff to enhance the industrial application of the results of their projects.
- Assist the scientific staff to attract financial resources (European, National, regional, and industrial calls).
- Disseminate information on calls to scientific staff.
- Advisor on IMSE strategic plans.
- Attend forums for the dissemination of calls.

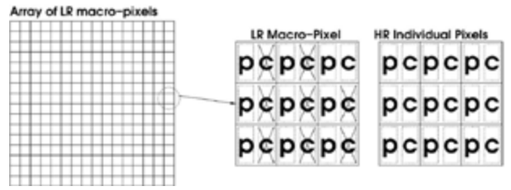
New Patent Application in 2024

Sensitive Dynamic Vision Sensor (sDVS) and Method for vision sensing

A sensitive DVS and method wich allows to perform foveation, computing temporal contrast on pixels for low and high resolution simultaneously.

Ideal for applications requiring both high-speed motion detection and power efficiency, such as autonomous vehicles, robotics and advanced surveillance systems.

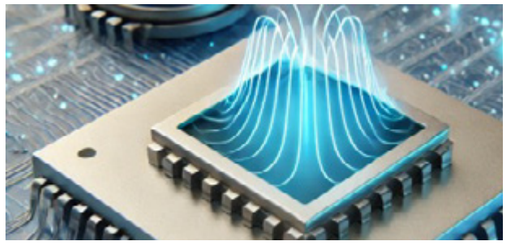
Status	**Patent pending**
Priority	**02/07/24**
Inventors	**Linares Barranco, Bernabé; Serrano Gotarredona, Teresa**
Patent Holder	**Spanish National Research Council**



Method and device for monitoring the output signal of nano-oscillators

This technologie introduces a compact device and a simplified method for monitoring nano-oscillators while enhancing performance. By capturing the output of nano-oscillators directly on-chip, both size and energy consumption are significantly reduced, eliminating the need for external radio frequency detectors.

It is also scalable and versatile, making it adaptable for

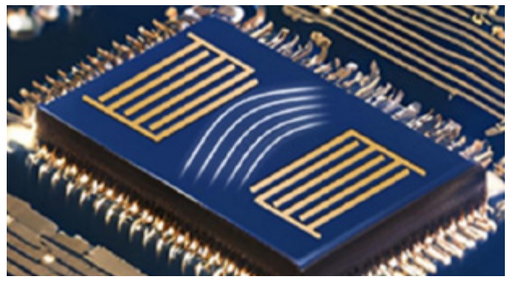


neuromorphic computing applications or small-scale magnetic sensors.

Status	**Patent pending**
Priority	**23/07/24**
Inventors	**Fiorelli Martegani, Rafaella Bianca; Peralías Macías, Eduardo**
Patent Holder	**Spanish National Research Council and University of Seville**

Acousto-Optic System & Method for generating PUFs

This method to generate strong physical unclonable functions (PUFs) uses acousto-optic systems. In this system the acousto-optic medium modulates an optical beam to generate multiple patterns used to probe a PUF based in optical scattering. This system allows to reduce complexity while maintaining high integrability and reliability.

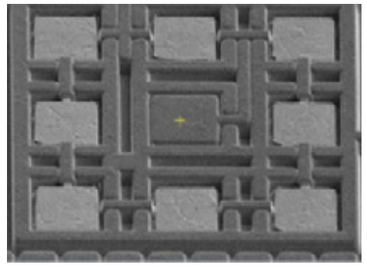


Multiple challenge-response pairs can be generated by varying the properties of the acoustic signal or by using multiple acousto-optic mediums could arranged sequentially. In addition, this acousto-optic system can be implemented as a photonic integrated circuit (PIC), enabling its miniaturisation and integration in Internet-of-Things (IoT) devices.

Status	**Patent pending**
Priority	**31/05/24**
Inventors	**Martín Sanchez, David; Brox Jiménez, Piedad**
Patent Holder	**Spanish National Research Council**

Published and Granted Patents

Semiconductor Particle Detector Device



This radiation-resistant semiconductor device is integrated into standard CMOS manufacturing technology. It acts as an active pixel in imaging detectors. It is capable of capturing images by detecting charged particles with energies in the range of 1 to 10 KeV. Its operation is based on measuring the electrostatic charge generated in a capacitor when it is irradiated by radiation. It uses MiM capacitors available in standard CMOS processes. The device can detect and measure both the sign and variations of the charge induced on a floating metal electrode. The pixel distribution allows the spatial distribution of the ionizing radiation flux to be measured.

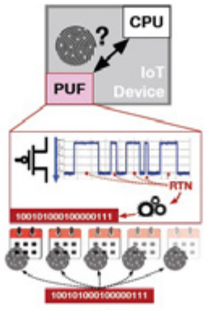
Status	**Patent pending**
Priority	**14/07/23**
Inventors	**Carmona Galán, Ricardo; Leñero Bardallo, Juan Antonio; Johanny Sáenz Noval, Jorge y Cervera Gontard, Lionel**
Patent Holder	**Spanish National Research Council, University of Seville and University of Cadiz**

Method and Hardware for single-shot simultaneous AE and HDR imaging

This sensing method for simultaneous realization of auto-exposure (AE) and high dynamic range (HDR) during image capture. Hardware implementation based on pixel array circuitry that automatically adjusts its response to the ambient illumination and fits the radiance map of the scene into the available signal range. Linear sensor response for low levels of light intensity and non-linear sensing response for high levels of light intensity – "low" and "high" relative to the ambient illumination. No extra time apart from the photo-integration interval needed to generate a HDR image. Arbitrary radiance maps can be accommodated into the available signal range. Asynchronous operation of the proposed circuitry once the pixels are reset, requiring no external control.

Status	**Patent pending**
Priority	**26/10/23**
Inventors	**Carmona Galán, Ricardo; Fernández Berni, Jorge y Lamouraa Sedlackova, Yassine**
Patent Holder	**Spanish National Research Council and University of Seville**

Method and device for PUF based on RTN



CSIC and the University of Seville have developed a method and device for a Physical Unclonable Function (PUF) whose source of entropy comes from the phenomenon known as Random Telegraph Noise (RTN). The key element that differentiates the present invention from similar inventions that might use this phenomenon is the fact that it uses a metric that can capture, in a comprehensive manner, the amount of RTN present in each transistor. This invention allow that a PUF response can be obtained and can be used, for example, to authenticate any hardware element to which an instance of the PUF device is bound.

Status	**Spanish Patent and PCT granted**
Priority	**18/04/22**
Inventors	**Roca Moreno, Elisenda; Castro López, Rafael; Brox Jiménez, Piedad; Camacho Ruiz, Eros; Fernández Fernández, Francisco Vidal**
Patent Holder	**Spanish National Research Council and University of Seville**

Computer-implemented methods for post-quantum protection of information and for post-quantum secure information matching and cryptographic systems to perform the computer-implemented methods

Computer-implemented methods for post-quantum protection of information and for post-quantum secure information matching and cryptographic systems to perform the computer-implemented methods

The present invention relates to post-quantum cryptographic methods for protecting sensitive information and matching the protected information. Sensitive information 10 can be represented by noisy data, in the sense that the data associated with identical sensitive information can show some differences among them when they are measured at different times. An example of noisy data is the data obtained from measurements of persons' and things' traits that are univocally associated with their physical entities, such as persons' biometric data.

The present invention relates to post-quantum cryptographic methods for protecting sensitive information and matching the protected information. Sensitive information 10 can be represented by noisy data, in the sense that the data associated with identical sensitive information can show some differences among them when they are measured at different times. An example of noisy data is the data obtained from measurements of persons' and things' traits that are univocally associated with their physical entities, such as persons' biometric data.

Status	**European Patent published**
Priority	**29/04/22**
Inventors	**Baturone Castillo, Mª Iluminada; Arjona López, María Rosario; López González; Paula; Román Hajderek, Roberto**
Patent Holder	**University of Seville**

Status	**European Patent published**
Priority	**29/04/22**
Inventors	**Baturone Castillo, Mª Iluminada; Arjona López, María Rosario; López González; Paula; Román Hajderek, Roberto**
Patent Holder	**University of Seville**

Pixel for DVS vision sensors with one or more photodiodes operating in photovoltaic regime

Csic and the University of Seville have developed a new Pixel arquitecture for DVS vision sensors with one or more photodiodes operating in photovoltaic regime. In this Pixel arquitecture, type "Dinamic Vision Sensor", its generated outputs pulses when the pixel detects temporary lighting variations. Its utilice several photodiodes, operating in photovoltaic region, like photoreceptors. The anode of this photodiodes can be directly connected to a buffer or voltage follower, whithout the necesity of using a logarithmic photoreceptor, reducing the dimensions of pixel respect other existing arquitectures.

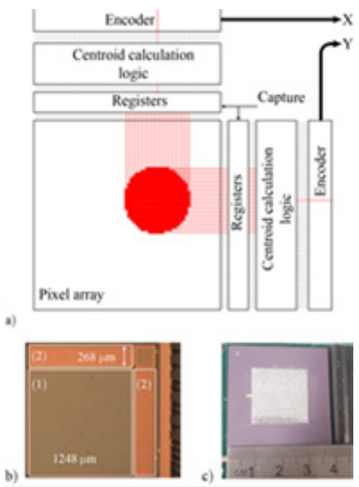
Status	**PCT published**
Priority	**27/10/22**
Inventors	**Leñero Bardallo, Juan Antonio; Rodríguez Vázquez, Ángel y Fernández Peramo, Pablo**
Patent Holder	**University of Seville**

Electronically foveated dynamic vision sensor

CSIC and the University of Seville have developed an electronically foveated dynamic vision sensor that operates at a low resolution by default, being able to activate high resolution only when it detects an area of interest. This is a very significant novelty since it allows lower energy consumption, less information and a lower subsequent computational load than a regular dynamic vision sensor.

Status	**Patent published**
Priority	**4/10/21**
Inventors	**Linares Barranco Bernabé; Serrano Gotarredona, María Teresa**
Patent Holder	**Spanish National Research Council and University of Seville**

Low-Power asynchronous solar sensor



CSIC and the University of Seville have designed an asynchronous solar sensor with important advantages in front of all existing comercial solar sensors: it significantly reduces power consumption by operating the diodes in the photovoltaic region, it has a response time several orders of magnitude faster, and it calculates the coordenates of the centroid of the pixel region inside the chip, requiring no post-processing of the sensor data.

Status	**Spanish, European and E.E.U.U patent granted**
Priority	**4/03/21**
Inventors	**Gómez Merchán, Rubén; Leñero Bardallo, Juan Antonio; Rodríguez Vázquez Ángel**
Patent Holder	**University of Seville and Spanish National Research Council**

EXTERNAL LIAISON

AWARDS & RECOGNITION

Two IMSE researchers among the winners at the 57th edition of ISCAS

IMSE-CNM researchers Gustavo Liñán-Cembrano and José Manuel de la Rosa have been awarded third prize in the "Best Live Demo" category at the 57th edition of the International Symposium on Circuits and Systems (ISCAS).

Alberto Patiño, a first prize winner at ISCAS 2024

Alberto Patiño Saucedo, postdoctoral researcher at the Instituto de Microelectronica de Sevilla (IMSE-CNM), has been awarded best paper by the Neural Systems and Applications Technical Committee of the IEEE Circuits and Systems Society (CAS). It was presented at this year's ISCAS Congress in Singapore.

The IMSE, awarded with the ASPIRA MaX CSIC distinction of excellence

On this occasion, 40 new Josefa Barba distinctions were awarded to CSIC Institutes and Centres (ICUs), including the Institute of Microelectronics of Seville (IMSE-CNM).

US professor and IMSE researcher Ángel Rodríguez Vázquez receives the Fama Award for his research and transfer career in the area of Engineering and Architecture

The University of Seville held the Fama Awards ceremony for research career on Tuesday 19 March 2024. On this occasion, the awards corresponding to the 2021-22 and 2022-23 editions were presented.

Piedad Brox Jiménez was awarded by the Technological University of Havana 'José Antonio Echeverría', CUJAE in the special category of Visiting Professor

2 IMSE researchers in the top 2% Stanford Ranking 2024

IMSE researchers Teresa Serrano and Bernabé Linares-Barranco have been included in this prestigious list.

OUTREACH

VISITING IMSE

A visit to the IMSE offers students, teachers, and the public in general an opportunity to obtain first-hand knowledge about the world of research and development in modern microelectronics. Visiting our facilities will certainly be of interest to anyone fascinated by science and technology, and also to those who would like to know exactly what kind of research is carried out in Andalusia and how it is done.

The visit is particularly recommended for high school students and students on professional training courses specializing in science and technology (electronics, IT, etc.).

To visit the IMSE, please contact us

visitas@imse-cnm.csic.es

+34 954 466 666.

TALKS

Danilo Demarchi visits the IMSE to discuss innovation in agri-food systems

The Italian professor gave a talk on the modernisation of the links in the food chain on 25 June.

European Researchers' Night

Part of the IMSE team was present once again at the European Researchers' Night, held on Friday 27 September, 2024

SOCIAL MEDIA

BLOGS & PRESS HIGHLIGHTS

SOscillatory Neural Networks: Tuning Artificial Intelligence

Oscillatory neural networks represent an exciting step forward in our journey towards understanding and emulating the complexity of the human brain, and their impact promises to be profound and long-lasting.

Source: **elDiario.es**

https://www.eldiario.es/andalucia/la-cuadratura-del-circulo/redes-neuronales-oscilatorias-sintonia-inteligencia-artificial_132_10881672.html

The PCT Cartuja de Sevilla, a benchmark in microelectronics

Three companies from the park participate in the Usechip Chair of the US, together with the School of Engineering and the Institute of Microelectronics The aim is to combat supply crises and avoid dependence on other markets.

Source: **Diario de Sevilla**

https://www.diariodesevilla.es/sevilla/pct-cartuja-sevilla-referente-microelectronica_0_2002317338.html

INSTITUTO DE MICROELECTRÓNICA DE SEVILLA

Centro Nacional de Microelectrónica

C/ Américo Vespucio
(Intersection with Leonardo Da Vinci)
PCT Cartuja: 41092 - Seville, Spain

Phone: +34 95 446 66 66

Fax: +34 95 446 66 00

www.imse-cnm.csic.es