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Paper title:

Improving delay-noise trade-off of dynamic gates for fine-grained pipelined applications

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session 6A. Analog Circuits Design 2
room: Zarautz
chairs: -

12:00 – 13:20

Implementation of two stage CMOS op-amp with very low open loop DC gain based on the QFG technique

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Input DC offset voltage in amplification stages is a critical issue in applications such as biomedical devices or direct-conversion communication receivers, where offsets of the same amplitude of the signal or even higher can exist. A simple structure based on Quasi-Floating Gate (QFG) transistors that reduces the DC gain of amplifiers is proposed in this work. It consists of a frequency-variable active load, whose effective output resistance is very low at DC and reaches its conventional high value at higher frequencies, affecting minimally the amplifier frequency response. The proposed technique has been applied to a classical two-stage Miller operational amplifier. Post-layout Cadence post-layout simulation results in 0.5µm technology are provided to show the improvement of the presented technique with respect to the conventional configuration.

A Study on the Offset Voltage of Dynamic Comparators

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Dynamic latched comparators are most used in analog-to-digital converters. In this paper expressions for the calculation of the offset voltage for two most used topologies are derived. These expressions corroborate previously stated results with analytical support as well as providing useful insight for the design of these comparators by analyzing the influence of each transistor pair individually. The results are validated by Monte Carlo simulations considering all the comparators in the input range of a Flash ADC using a 130nm CMOS Technology.

Test of Dual Axis Accelerometers Based on Specifications Compliance

Álvaro Gómez-Pau, Luz Balado and Joan Figueras
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Testing microelectromechanical systems (MEMS) devices is a challenging and time consuming task demanding high amount of resources. Devices targeting safety critical applications need to be efficiently tested in order to deliver reliable units to the market. MEMS systems require non electrical excitations inherent to their transduction functions what difficults even more the testing procedure. In this work, an accelerometer testing technique using octrees to encode the specifications compliance region is presented. The test proposal is based on the application of two phases, namely, training and testing. In the former phase, the acceptance region is generated according to device specifications and encoded using octrees. In the testing phase a novel test strategy is applied to a candidate device taking advantage of the benefits of evaluating octree structures. The method is applied to test dual axis accelerometers under parametric defects with encouraging results. Incurred test escapes and test yield loss as a function of the number of bits used to encode the octree have been statistically evaluated.

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Dynamic logic is well suited to implement very fine-grained pipelining for high performance functional units and has been successfully applied in commercial applications. Technology scaling and current increasing frequency targets have augmented the main problems exhibited by conventional dynamic gates topologies: larger leakage and coupling leading to higher noise susceptibility, logic design constrained by their functional limitation, being able to implement only non inverting functions and the labor-intensive design required due to timing challenges of fine grained pipelines used for high through-output. Development of novel topologies aiming to cope with all these challenges is an area of active research. In this paper, we describe a novel topology that addresses all the above stated problems. The proposed gate implements inverting functionalities, exhibits very competitive delay-noise tradeoffs and it is well suited to implement building blocks with function-independent delays which can simplify design. Unlike previous reported solutions, it is the gate static output stage which is modified. The novel topology is analyzed and evaluated, and a gate per phase Carry Look Ahead adder is designed as an application example.