ETS '09

IEEE
Celebrating 125 Years
of Engineering the Future

14th European Test Symposium

Final program

NH Central Convenciones Hotel

Sevilla, Spain

May 25-29, 2009

CSIC

IEEE computer society

tttc

Foreword

On behalf of the Steering and Program Committees, we would like to welcome you to the European Test Symposium 2009 (ETS'09), the largest event in Europe that is entirely devoted to presenting and discussing trends, emerging results, hot topics, and practical applications in the area of electronic-based circuit and system testing. ETS'09 is the 14th edition of this symposium, and it is held in Seville, a nice city with an important monumental and artistic heritage, located in the southwest of Spain.

ETS continues its well-established format with one day of tutorials, a three-day technical program, and an attractive social event. The symposium's technical program consists of two plenary keynote addresses, technical paper presentations in three parallel sessions, four embedded tutorials, poster sessions, one special session and two panels. Several test-related fringe events complete the "European Test Week," which includes the Workshop on Impact of Low Power Design on Test and Reliability (LPonTR'09).

ETS'09 received a large number of contributions from all over the world, submitted to the scientific track, workshop track (including emerging ideas and case studies), vendor sessions and special sessions. All submissions underwent a rigorous review process. For the scientific and workshop tracks, each paper has been reviewed on average by 6~8 reviewers. At a full-day TPC meeting, held on February 6, 2009 at Lisbon, Portugal, all papers were discussed and evaluated. Based on the reviews and the discussions, 23 scientific track papers were selected for inclusion in the ETS'09 Formal Proceedings. In addition, 8 vendor session presentations were selected; most of these have corresponding papers in the ETS'09 Electronic Symposium Digest of Papers. Finally, 35 submissions were selected for poster presentations.

The European Test Symposium is the achievement of the contributions of many volunteers, who give generously their time to contribute to the success of the symposium. We would like to thank all for their efforts. We are confident that you will find ETS'09 a productive and exciting experience, and would like welcome you to Seville.

J.L. Huertas
O. Novak
General Co-Chairs

J. P. Teixeira
Program Chair

E. Gramatova
Vice Program Chair

C. Metra
Publication Chair

Presentations are marked as follows:

F formal

I informal

V vendor

Committees

Organizing Committee

General Co-Chair	J. L. Huertas - IMSE-CNM (E)
General Co-Chair	O. Novak - Czech Technical Univ. (CZ)
Program Chair	J. P. Teixeira - IST/INESC-ID (P)
Vice Program Chair	E. Gramatova - Slovak Acad. of Sc. (SK)
Local Organization Chair	A. Rueda - IMSE-CNM/Univ. Sevilla (E)
Panel Chair	H. J. Wunderlich - Univ. Stuttgart (D)
Industrial Relations Chair	P. Harrod - ARM Ltd. (UK)
Publication Chair	C. Metra - Univ. Bologna (I)
Tutorials Chair	P. Girard - LIRMM (F)
Embedded Tutorials Chair	P. Prinetto - Pol. Torino (I)
Fringe Workshops Chair	B. Al-Hashimi - Univ. Southampton (UK)
Ph. D. Forum Chair	I. Polian - Univ. Freiburg (D)
Asian Liaison	S. Kajihara – Kyushu IT (J)
Pacific Liaison	A. Osseiran – Edith Cowan Univ. (AUS)
North-American Liaison	A. Singh – Auburn Univ. (USA)
Latin-American Liaison	L. Carro – UFRGS (BR)

Local Organizing Committee

IMSE-CNM, Univ. de Sevilla (E)

Local Chair	A. Rueda
Proceedings	G. Huertas
Local Arrangement	D. Vázquez
Registration	E. Peralías, A. Acosta
Audio-Visual	G. Leger
Web	S. Sánchez

Steering Committee

Chair	H. J. Wunderlich - Univ. Stuttgart (D)
	B. Al-Hashimi - Univ. Southampton (UK)
	B. Becker - Univ. Freiburg (D)
	J. Figueras - Univ. Pol. de Catalunya (E)
	C. Landrault - LIRMM (F)
	E. J. Marinissen - NXP Semicond. (NL)
	P. Muhmenthaler - Infineon (D)
	Z. Peng - Linköping Univ. (S)
	P. Prinetto - Pol. Torino (I)
	M. Renovell - LIRMM (F)
	M. Sonza Reorda - Polit. di Torino (I)
	J. P. Teixeira - IST/INESC-ID (P)
	Y. Zorian - Virage Logic (USA)

Program Committee

Topic chairs

B. Becker - Univ. Freiburg (D)
S. Hellebrand - Univ. Paderborn (D)
H. Kerkhoff - Univ. Twente (NL)
E. Larsson - Linköping Univ. (S)
R. Leveugle - TIMA (F)
P. Muhmenthaler - Infineon (D)
N. Nicolici - McMaster Univ. (CAN)
M. Renovell - LIRMM (F)

Members

E. Aas - Norvegian Univ. of Science (N)
M. Abadir - Motorola (USA)
R. Aitken - ARM Artisan (USA)
Z. Al-Ars - Delft Univ. of Technology (NL)
D. Appello - STMicroelectronics (I)
F. Azais - LIRMM (F)
M. Azimane - NXP Semiconductor (NL)
L. Balado - Univ. Politècnica de Catalunya (E)
A. Benso - Politecnico di Torino (I)
G. Carlsson - Ericsson (S)
K. Chakrabarty - Duke Univ. (USA)
W. Daehn - HS Magdeburg-Stendal (D)
R. Dorsch - IBM Entwicklungs GmbH (D)
M. L. Flottes - LIRMM (F)
H. Fujiwara - NAIST (J)
F. Fummi - Univ. of Verona (I)
D. Gizopoulos - Univ. of Piraeus (GR)
E. Gramatova - Slovak Academy of Sc. (SK)
S. Hamdioui - Delft Univ. of Technology (NL)
M. Hirech - Synopsys (USA)
A. Hlawiczka - Silesian Univ. of Tech. (PL)
M. S. Hsiao - Virginia Tech (USA)
P. Hughes - ARM (UK)
A. Ivanov - Univ. of British Columbia (CAN)
S. Kajihara - Kyushu Institute of Tech. (J)
R. Kapur - Synopsys (USA)
A. Krasniewski - Warsaw Univ. (PL)
B. Kruseman - NXP Research (NL)
S. Kundu - Univ. of Massachusetts (USA)
M. Lubaszewski - UFRGS (BR)
Y. Makris - Yale Univ. (USA)
H. Manhaeve - QStar Test (B)
E.J. Marinissen - NXP Semiconductor (B)
P. Maxwell - Micron Technology (USA)
L. Miclea - Tech. Univ. of Cluj-Napoca (RO)
S. Mir - TIMA CMP (F)
S. Mitra - Stanford Univ. (USA)
Y. Miura - Tokio Metropolitan Univ. (J)
F. Novak - Jozef Stephan Institute (SLO)
O. Novak - TU Prague (CZ)
A. Orailoglu - UCSD (USA)
S. Ozev - Duke Univ.(USA)
A. Pataricza - Budapest Univ. of TE (H)
Z. Peng - Linköping Univ. (S)
F. Poehl - Infineon Technologies (D)
I. Polian - Freiburg Univ. (D)
I. Pomeranz - Purdue Univ. (USA)
J. Raik - Tallinn Univ. (EE)
J. Rajski - Mentor Graphics (USA)
A. Richardson - Lancaster Univ. (UK)
J. Rivoir - Agilent Technologies (D)
B. Rouzeyre - LIRMM (F)
A. Rubio - Univ. Politècnica de Catalunya (E)
A. Rueda - IMSE-CNM/Univ. Sevilla (E)
K. K. Saluja - Madison Univ. (USA)
P. Sanchez - Univ. de Cantabria (E)
S. Sattler - Infineon Technologies (D)
J. Segura - Univ. de les Illes Balears (E)
M. Sonza Reorda - Politecnico di Torino (I)

Members (continuation)

J. P. Teixeira - IST/INESC-ID (P)
N. Touba (USA) - Univ. of Texas
J. Tyszer (PL) - Poznan Univ.
R. Ubar (EE) - Tallin Univ.
B. Vermeulen (NL) - NXP Research
C. Wegener (D) - Infineon Technologies
X. Wen (J) - Kyushu Institute of Tech.
C. W. Wu (TW) - National T-H Univ.
M. Zwolinski (UK) - Univ. of Southampton

TTEP Tutorials 9:00 – 13:00 and 14:30 – 17:30

Alanda Room

The tutorials of ETS'09 are part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2009.

Tutorial 1

Advanced Topics and Recent Advances in Silicon Debug and Diagnosis

Srikanth VENKATARAMAN, Intel Corp. (USA)
Miron ABRAMOVICI, Dafca Corp. (USA)
Robert AITKEN, ARM Artisan (USA)

Summary: The increasing design complexity along with the emergence of new failure mechanisms in the nanometer regime has significantly increased the complexity of verification, validation and manufacturing ramp of ICs. When pre-silicon verification and validation uncovers design bugs, the process of diagnosing and debugging these issues is called design error diagnosis. From the time a new chip comes back from the fab until high-volume production can start, the chip goes through functional silicon validation and debug to make sure it is free of design errors, and defect diagnosis and failure analysis to solve yield problems. These activities, referred to as silicon debug and diagnosis, have become the most time-consuming phase in the development cycle of a new design, increasing to about 33% of the total time. This is a consequence of the increasing design complexity, along with the emergence of new failure mechanisms in nanometer technologies. Long time-to-volume and low manufacturing yield have a great detrimental impact on the economic viability and the overall success of a product. This tutorial covers the state of the art and the full spectrum of topics in silicon validation and debug and defect diagnosis ranging from the basic concepts to advanced applications and new DFD techniques. We will also describe successful debug and diagnosis methods used in real industrial products, industrial experiences, and case studies. Finally we will discuss future directions and challenges.

OUTGROWING YOUR TEST NEEDS?

Design-for-Test | Mentor Graphics industry-leading silicon test solutions offer the highest test compression levels enabling the highest test quality for our customers. For more information on the TestKompress® embedded compression product, winner of the *Test & Measurement World* 2009 Test of Time award, and the rest of Mentor's test solutions visit www.mentor.com/silicon_test

Mentor Graphics®

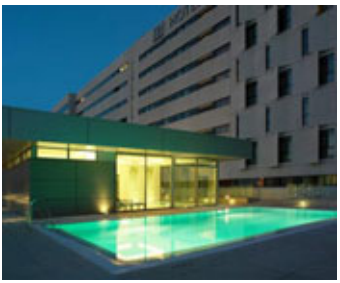
THE EDA TECHNOLOGY LEADER

NH Hotel terrace

Welcome Reception

20:00 – 22:00

The welcome reception will be held at the NH Central Convenciones Hotel.



NH Central Convenciones Hotel

Address: Avda. Diego Martinez Barrio, 8 41013 Seville (Spain)
Tel: +34 954548500
e-mail: nhcentralconvenciones@nh-hotels.com

Session 1 — 8:30 – 10:30

Plenary Opening — 8:30 – 9:10

Moderator: *Bashir Al-Hashimi, Southampton Univ. (UK)*

Welcome Address 8:30 – 8:40
Jose Luis HUERTAS, IMSE-CNM (E) - ETS'09 General Chair

Technical Program Overview 8:40 – 8:50
J. Paulo TEIXEIRA, IST/INESC-ID (P) - ETS'09 Program Chair

Presentation of ETS'08 Best Paper Award 8:50 – 9:00
Patrick GIRARD, LIRMM (F) - ETS'08 Program Chair

TTTC Award Ceremony 9:00 – 9:10
Yervant ZORIAN, Virage Logic (USA) - TTTC Senior Past Chair

Keynotes — 09:10 – 10:30

Keynote 1 09:10 – 09:50

We have got compression, what next?

Janusz RAJSKI, Mentor Graphics Corp. (USA)

Abstract: Test compression is one of the fastest adopted DFT methodologies. It was commercially introduced eight years ago, and now it has become the mainstream DFT technology. Disruptive technology of this magnitude has impact that goes far beyond cost of manufacturing test. Test compression has changed competitive landscape, opened up completely new opportunities in product quality and yield management, and has redefined DFT technology roadmaps. It stimulates research and development activities in new areas that until now were considered not promising or not practical, enables quality of testing that was unachievable until now, accelerates adoption of new fault models that take into account physical data bases and timing information, and changes how fault diagnostics and yield learning are done in manufacturing environment.

There is a passionate debate in the professional community on the future of test compression. How scalable is it? How long will it keep up with the growing sizes of designs? What is the maximum achievable compression? How can we accommodate power constraints? What is its impact on our ability to perform diagnosis in volume production? Was it a one time deal or is it scalable solution that will be around for many generations of semiconductor technologies? Some voices focus on opportunities, others point to limitations. Some arguments are grounded in engineering others resort to financial analysis. Many of the predictions are conflicting. The presentation will discuss many of these issues, new opportunities, new and not so new challenges, as well as future technology roadmaps.

Curriculum vitae: Janusz Rajski received the Ph.D. degree in electrical engineering from Poznań University of Technology, Poland, in 1982. In June 1984, he joined McGill University, Montreal, Canada, where he became Associate Professor in 1989. In January 1995 he accepted the position of Chief Scientist at Mentor Graphics Corporation, Wilsonville, Oregon. In 2002 he became Director of DFT Engineering.

His main research interests include design automation and testing of VLSI systems, design for testability, built-in self-test, and logic synthesis. He has published more than 180 research papers in these areas and is a co-inventor of 36 US and international patents. He is also the principal inventor of Embedded Deterministic Test (EDT™) technology used in the first commercial test compression product TestKompress®. He is co-author of *Arithmetic Built-In Self-Test for Embedded Systems* published by Prentice Hall in 1997.

He was co-recipient of the 1993 Best Paper Award for the paper on logic synthesis published in the *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, co-recipient of the 1995 and 1998 Best Paper Awards at the IEEE VLSI Test Symposium, co-recipient of the 1999 and 2003 Honorable Mention Awards at the IEEE International Test Conference, as well as co-recipient of the 2006 IEEE Circuits and Systems Society Donald O. Pederson Outstanding Paper Award recognizing the paper on embedded deterministic test published in the *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. In 2009 he received the Stephen Swerling Innovation Award from Mentor Graphics "for his breakthrough innovation, TestKompress, and his many contributions to revitalizing Mentor's DFT business to its current position as #1 test business in EDA".

Janusz was a guest co-editor of the June 1990 and January 1992 special issues of *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* devoted to the 1987 and 1989 International Test Conferences, respectively. In 1999, he was a guest co-editor of the special issue of the *IEEE Communications Magazine* devoted to testing of telecommunication hardware. He was also an associate editor for *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Computers,* and *IEEE Design and Test of Computers Magazine*. He has served on technical program committees of various conferences including the IEEE International Test Conference and the IEEE VLSI Test Symposium. In 2007 he served as a Program Chair for ITC.

Keynote 2 09:50 – 10:30

Something I Always Wanted to Know About Test, But Was Afraid to Ask

Christian LANDRAULT, LIRMM (France)

Abstract: As pinpointed in the last ITRS report and also clearly highlighted in the past years test conference programs, the overall mission of manufacturing test is continuously shifting from its "screening defects" basic and primary objective towards more subtle and secondary goals constituted for example by reliability aspect and yield learning. Just after his retirement, the author examines these new testing opportunity and will try to give directions to all what he missed and failed to do in his research career.

Curriculum vitae: Christian Landrault was born in Orléans (France) on December 8, 1946. He received the Engineering degree from the Higher National School for Aeronautical Constructions (ENSICA), Toulouse, France in 1970, the Doctor in Engineering degree in Automatic Control, and the Doctor es-sciences degree in Computer Science from the National Polytechnic Institute of Toulouse, in 1973 and 1977, respectively. From 1970 to 1980, he worked at "Laboratoire d'Automatique" et d'Analyse des Systèmes (LAAS, Toulouse) on self checking circuits, dependability architecture and dependability evaluation of digital systems. In 1980, he joined the Laboratory of Informatics, Robotics and Microelectronics of Montpellier (LIRMM) where he is currently a "Directeur de Recherche at CNRS (National Scientific Research Center)."

C. Landrault's scientific interests include fault modelling, digital and memory testing, fault simulation, ATPG, design for testability and BIST. Christian Landrault has authored or co-authored over 150 papers for international and national journals and conferences and has supervised 27 PhD dissertations on Electronic Design Automation. Dr. Landrault is serving most of the test conference Program Committees (ITC, VTS, ICCAD, DATE, ATS, ETS) and is a member of the editorial board of the Journal of Electronic Testing and Applications. Dr. Landrault has founded the European Test Workshop, which became the European Test Symposium in 2004 with Dr. Landrault as steering committee chairperson. Dr. Landrault is a Golden Core Member of the IEEE Computer Society. He is now on retirement and his main interests have shifted to fly fishing and mushroom picking.

Session 2

10:30 – 11:30

Poster Session I

Testing of Strongly-Indicating Asynchronous Datapaths
Deepali KOPPAD, University of Edinburgh (UK)

A Methodology to Evaluate Transient-Fault Effects on Asynchronous and Synchronous Circuits
Rodrigo POSSAMAI BASTOS, TIMA (France); Yannick MONNET, TIEMPO (France); Gilles SICARD, TIMA (France); Fernanda KASTENSMIDT, UFRGS (Brazil); Marc RENAUDIN, TIEMPO (France); Ricardo REIS, UFRGS (Brazil)

On-line error detection of a compact 32 bit hardware AES implementation
Uros LEGAT, Anton BIASIZZO, Franc NOVAK, Jozef Stefan Institute (Slovenia)

A High Precision Analog Signal Generator Design for ADC BIST
Vincent O´BRIEN, Brendan MULLANE, Thomas FLEISCHMANN, C. MacNAMEE, Univ. of Limerick (Ireland)

Deterministic Scan-chain Diagnosis for Intermittent Faults
Dan ADOLFSSON, NXP Semiconductors (The Netherlands); Joanna SIEW, Philips Applied Technologies (The Netherlands); Erik LARSSON, Linkoping University (Sweden); Erik Jan MARINISSEN, IMEC (Belgium)

A SBST Methodology for applying March Tests to Processor Cache Memory Tags
Georgios A. THEODOROU, Nektarios KRANITIS, Antonis PASCHALIS, Univ. of Athens (Greece); Dimitris GIZOPOULOS, Univ. of Piraeus (Greece)

Analysis of Resistive-Bridging Defects in SRAM Core-Cell: Impact within the Core-Cell and in the Memory Array
Renan ALVES FONSECA, Alberto BOSIO, Luigi DILILLO, Patrick GIRARD, Serge PRAVOSSOUDOVITCH, Arnaud VIRAZEL, LIRMM (France); Nabil BADEREDDINE, Infineon Technologies (France)

Forward-Looking Reverse Order Fault Simulation for n-Detection Test Sets
Irith POMERANZ, Purdue University (USA); Sudhakar REDDY, University of Iowa (USA)

Design-for-Debug of Mixed Signal Cores
Nuno DIAS, Ângelo MONTEIRO, IST/INESC-ID (Portugal); Marcelino SANTOS, Gabriel SANTOS, SiliconGate (Portugal); J. Paulo TEIXEIRA, IST/INESC-ID (Portugal)

Almenara Room

Session 3A

11:30 – 13:00

Internal Testing of Mixed- Signal Cores

Moderators: *Florence AZAIS, LIRMM (France)*
Salvador MIR, TIMA (France)

F **Testing of High Resolution ADCs Using Lower Resolution DACs Via Polynomial Transfer Function Estimation**
Sehun KOOK, V. NATARAJAN, Abhijit CHATTERJEE, Georgia Tech. (USA); Shalabh GOYAL, Le JIN, National Semiconductor Corp. (USA)

I **Digital Signature Generator for Mixed-Signal Testing**
Ricard SANAHUJA, Alvaro GÓMEZ, Luz BALADO, Joan FIGUERAS, Univ. Pol. de Catalunya (Spain)

I **Simulations and Experimental results of INL Testing of 16-b A/D Converters without an Accurate Test Stimulus**
Esa KORHONEN, Juha KOSTAMOVAARA, University of Oulu (Finland)

Session 3B

11:30 – 13:00

Avenida Room

Debug and Validation

Moderators: *Rob AITKEN, ARM (USA)*
Miron ABRAMOVICI, Dafca Corp. (USA)

F **Speed Path Debug Using At-Speed Scan Test Patterns**
Ruifeng GUO, Wu-Tung CHENG, Kun-Han TSAI, Mentor Graphics Corp (USA)

F **Resource-Efficient Programmable Trigger Units for Post-Silicon Validation**
Ho Fai KO, Nicola NICOLICI, McMaster University (Canada)

I **The Role of Mutation Analysis for Property Qualification**
Luigi di GUGLIELMO, Franco FUMMI, Graziano PRAVADELLI, Università di Verona (Italy)

Session 3C

11:30 – 13:00

Alanda Room

Vendor Session 1

Moderators: *Marcelino SANTOS, IST/INESC-ID & SiliconGate (Portugal)*
Regis LEVEUGLE, TIMA (France)

V **Advanced DFT Techniques for Deep Sub-micron Design**
Nikolaus MITTERMAIER, Synopsys (USA)

V **Emerging Standards for Digital Test and Diagnosis**
Geir EIDE, Mentor Graphics Corporation (USA)

V **The ARM Standardized MBIST Port**
Teresa McLAURIN, ARM (USA)

OPTIMAL TEST
MASTERING TEST MANAGEMENT

Early Detection Solution Improves
Profitability across Global Test Operations

Come hear OptimalTest speak on May 26th
14:30 – 16:00 Session 4C: Vendor Session 2

BEST IN TEST 2009
TEST & MEASUREMENT WORLD

Comprehensive Solutions, Actionable Data.
Adapt. Evolve. Win.

Almenara Room

Session 4A

14:30 – 16:00

Power Issues During Test

Moderators: *Sebastian SATTLER, Friedrich-Alexander Univ., Erlamgen-Nürnberg, (Germany)*
Patrick GIRARD, LIRMM (France)

F **On Minimization of Peak Power for Scan Circuit during Test**
Jaynarayan TUDU, Indian Institute of Science (Bangalore, India); Erik LARSSON, Linkoping Univ. (Sweden); Virendra SINGH, Indian Institute of Science (Bangalore, India); Vishwani AGRAWAL, Auburn University (USA)

I **Understanding Power Issues during ATPG Using Volume Diagnosis**
Vincenzo TANCORRE, Patrice DORIOL, Roberto MATTIUZZO, STMicroelectronics (Italy); S Bahl, A. Garg, STMicroelectronics (India); Salvatore TALLUTO, M. HALL, C. SUZOR, Synopsys Inc. (USA); Davide PANDINI, STMicroelectronics (Italy); R. KAPUR, Synopsys Inc. (USA); Davide APPELLO, STMicroelectronics (Italy)

I **Built-In Test Driven Power Aware Self Tuning of Wideband RF Devices**
Shyam Kumar DEVARAKOND, Vishwanath NATARAJAN, Shreyas SEN, Abhijit CHATTERJEE, Georgia Institute of Technology (USA)

Session 4B

14:30 – 16:00

Avenida Room

Self-test and Test Throughput

Moderators: *Cecilia METRA, Univ. of Bologna, Italy*
Gert JERVAN, Tallinn Univ. (Estonia)

F **Exploiting Thread-Level Parallelism in Functional Self-Testing of CMT Processors**
Andreas APOSTOLAKIS, Mihalis PSARAKIS, Dimitris GIZOPOULOS, Univ. of Piraeus (Greece); Antonis PASCHALIS, Univ. of Athens (Greece); Ishwar PARULKAR, Sun Microsystems (USA)

F **Doubling Test Cell Throughput by On-Loadboard Hardware, Implementation and Experience in a Production Environment**
Frank-Uwe FABER, Matthias BECK, Markus RUDACK, Olivier BARONDEAU, Infineon Technologies AG (Germany); Thomas RABENALT, MICHAEL GÖSSEL, Andreas LEININGER, University Potsdam (Germany)

F **Algorithms for ADC Multi-Site Test with Digital Input Stimuli**
Xiaoqin SHENG, Hans KERKHOFF, Univ. of Twente (The Netherlands); Amir C. ZJAJO, Guido GRONTHOUD, NXP Semiconductors (The Netherlands)

Session 4C

14:30 – 16:00

Alanda Room

Vendor Session 2

Moderators: *Nicola NICOLICI, McMaster Univ. (Canada)*
Zdenek KOTASEK, Brno Univ. of Technology (Czech Republic)

V **Early Detection Solution Improves Profitability across Global Operations**
Debbora AHLGREN, OptimalTest (Israel)

Test Program Maintenance and Optimization
Meir GELLIS, TestInsight, Ltd. (Israel)

Effectiveness of an RTL Design for Test Solution on an Industrial Test Case
Chouki AKTOUF, Ivano MIDULLA, DeFacto Technologies (France)

Session 5

16:00 – 17:00

Poster Session II

A Low-Cost on-chip Design Platform for static ADC Measurements
Brendan MULLANE, C. MacNAMEE, Vincent O´BRIEN, Thomas FLEISCHMANN, Univ. of Limerick (Ireland)

Early Pruning of Soft Errors and Transient Faults with Petri Nets
Paolo MAISTRI, Regis LEVEUGLE, TIMA Lab. (France)

An Efficient Approach to the Generation of Test Programs for Cache Controllers
Wilson-Javier PEREZ HOLGUIN, Universidad del Valle and Universidad Pedagógica y Tecnológica de Colombia (Colombia); Danilo RAVOTTO, Ernesto SANCHEZ, Matteo SONZA REORDA, Politécnico di Torino (Italy)

Test Generation and DFT Based on Partial Thru Testability
Nobuya OKA, Hiroshima City University (Japan); Chia Yee OOI, Universiti Teknologi Malaysia (Malaysia); Hideyuki ICHIHARA, Tomoo INOUE, Hiroshima City University (Japan); Hideo FUJIWARA, Nara Institute of Science and Technology NAIST (Japan)

Simulation Methodology for the Validation of Low Energy Particle Accelerators as Fault Injection Tools
Juan M. MOGOLLÓN, Rogelio PALOMO PINTO, Miguel A. AGUIRRE, Javier NÁPOLES, Hipólito GUZMÁN-MIRANDA, Univ. of Sevilla (Spain)

BISR Architecture and Methodology for Fault-Tolerant Embedded Memories
Nicholas AXELOS, Kiamal PEKMESTZI, National Technical University of Athens (Greece)

Towards an Integrated Environment to Enhance Yield Learning
Simona PAPPALARDO, ST Microelectronics (Italy)

Dynamic Interconnect Testing in Multi-Bus, Multi-FPGA Digital Systems
Carlos LEONG, Vasco BEXIGA, Pedro MACHADO, Isabel TEIXEIRA, João Paulo TEIXEIRA, IST/INESC-ID (Portugal)

System-Level Hardware-Based Protection Scheme against Memory Errors
Valentin GHERMAN, Samuel EVAIN, Mickaël CARTRON, Nathaniel SEYMOUR, Yannick BONHOMME, CEA, LIST (France)

Session 6A

17:00 – 18:00

Avenida Room

On-line Testing

Moderators: *Marie-Lise FLOTTES, LIRMM (France)*
Salvador BRACHO, Univ. of Cantabria (Spain)

F **Concurrent Self-Test with Partially Specified Patterns for Low Test Latency and Overhead**
Michael KOCHTE, Christian ZOELLIN, Hans-Joachim WUNDERLICH, Univ. of Stuttgart (Germany)

I **Low Cost On-Line Testing of the Scheduler of High Performance Microprocessors**
Cecilia METRA, Daniele ROSSI, Martin Eugenio OMAÑA, M. SANGIORGI, Univ. of Bologna (Italy); Abhijit JAS, Rajesh GALIVANCHE, Intel Corp. (USA)

ETS '09

Remember

F formal

I informal

V vendor

Alanda Room

Session 6B

17:00 – 18:00

Vendor Session 3

Moderators: *Erik Larson, Linkoping Univ. (Sweden)*
Matteo Sonza-Reorda, Polit. Torino (Italy)

V **Single Event Effects. A Test Strategy for New Technologies and Nowadays Needs**
Gonzalo FERNÁNDEZ, ALTER Technology Group (Spain)

V **Evaluation of Optoelectronic Components for Space Applications**
Juan BARBERO, Enrique CORDERO, Laura PEÑATE, Alina SPUMA, Javier PÉREZ, Sara DIAZ, ALTER Technology Group (Spain)

Avenida Room

Session 7A

18:00 – 19:30

Panel 1

Organizers: *Said HAMDIOUI, TU Delft (The Netherlands)*
Simona PAPPALARDO, ST Microelectronics (Italy)
Moderator: *Tom W. WILLIAMS, Synopsys (USA)*

Yield, Reliability, and Variability in the Nano-Era: Will Existing Approaches Survive?

Panelists: *Debbora AHLGREN, OptimalTest (Israel); Brady BENWARE, Mentor Graphics (USA); Teresa McLAURIN, ARM (USA); Udo SCHWALKE, Techn. University Darmstadt (Germany); Srikanth VENKATARAMAN, Intel (USA)*

Abstract: It is widely recognized that variability in device characteristics and the new failure mechanisms in the nano-technology era will severely impact the design, manufacturing, and testing of future chips. In addition, time-to-market and time-to-volume pressure have created major engineering challenges in rapid yield learning and guaranteeing the required quality and reliability.
The panel aims at gathering opinions on the different ways to deal with these challenges in order to survive the nano-era. Can we still rely on test data analysis to accurately predict the reliability of the manufactured chips? Can today's methodologies such as burn-in still be able to provide the required reliability? Can statistics provide the necessary information of the root cause of yield loss without performing the time-consuming physical failure analysis? Are existing test approaches still able to deliver the required product quality even if the failure mechanisms are shifting from permanent faults to intermittent and transient faults? Does the impact on memory differ from the impact on logic?

Session 7B

18:00 – 19:30

Panel 2

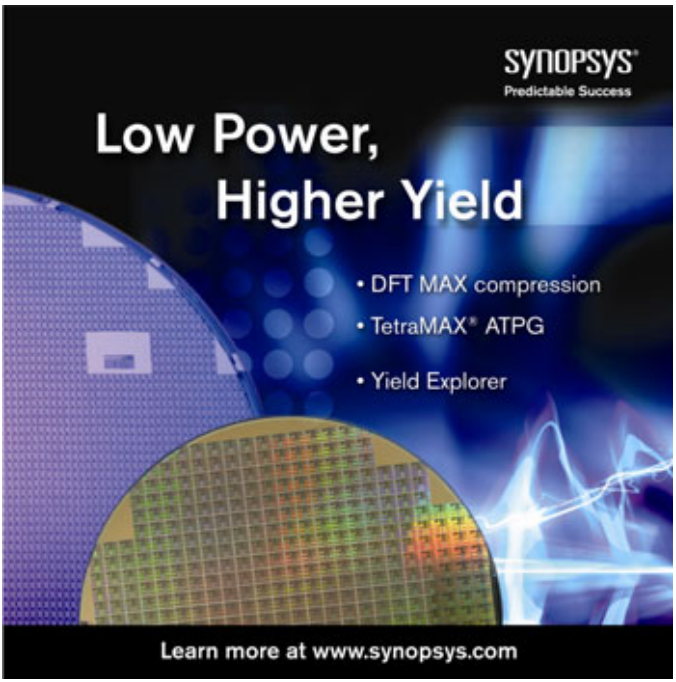
Organizer and Moderator: *Hans-Joachim WUNDERLICH Univ. Stuttgart (Germany)*

Extended Diagnosis Requirements in Automotive Applications

Panelists: *Davide APPELLO, STM (Italy); Stephen SUNTER, LogicVision (USA); Frank POEHL, Infineon (Germany); Sebastian SATTLER (Germany)*

Abstract: The cars of today show more and more functions and features implemented in hardware and software which were formerly realized by mechanics. In addition, a tremendous amount of new functionalities are added like automatic distance holding, road recognition or the complete infotainment which require a computing power formerly only seen in super computers. As a consequence, the gap between very mature technology for car microelectronics and most advanced technology for high performance computing is reduced year by year, and debug and diagnosis are now also severe challenges for the automotive industry.

Time consuming diagnosis procedures where car makers and different suppliers are involved may cause tremendous costs for delayed production or delivery, call for returns or repair. The session will discuss how design for test, embedded diagnosis or testability considerations and features at the ASIC level can help at system level.



Program at a glance

Monday, May, 25

ETS'09 Tutorials

9:00 – 13:00	**TTEP Tutorial 1** Advanced Topics and Recent Advances in Silicon Debug and Diagnosis

lunch

14:30 – 17:30	**TTEP Tutorial 1** Advanced Topics and Recent Advances in Silicon Debug and Diagnosis
20:00 – 22:00	**Welcome Reception** (NH Hotel terrace)

Tuesday, May, 26

ETS'09 Program At a Glance

8:30 – 10:30	**Plenary Opening Keynote Addresses**		
10:30 – 11:30	Session 2 - **POSTER I** and Coffee Break		
11:30 – 13:00	Session 3A Internal Testing of Mixed-Signal Cores	Session 3B Debug and Validation	Session 3C Vendor 1

lunch

14:30 – 16:00	Session 4A Power Issues During Test	Session 4B Self-test and Test Throughput	Session 4C Vendor 2
16:00 – 17:00	Session 5 - **POSTER II** and Coffee Break		
17:00 – 18:00	Session 6A On-line Testing	Session 6B Vendor 3	
18:00 – 19:30	Session 7A **Panel 1** Yield, Reliability and Variability in the Nano-Era	Session 7B **Panel 2** Extended Diagnosis Req. in Automotive Applications	

Program at a glance

Wednesday, May, 27

ETS'09
Program At a Glance

9:00 – 10:30	Session 8A Advanced Testing Mem., Power Trans. Microfluidic Syst.	Session 8B Recent Advances in ATPG	Session 8C Student's Forum
10:30 – 11:30	Session 9 - Coffee Break and **STUDENT'S POSTERS**		
11:30 – 13:00	Session 10A Advanced External Test of Mixed-Signal Cores	Session 10B Diagnosis and Dependability Analysis	Session 10C **Special** Soft Errors in Electronic Systems

lunch

14:30 – 15:30	Session 11A **Emb. Tutorial 1** Switching Noise and Process Var. Challenges in Delay Testing	Session 11B **Emb. Tutorial 2** Test Challenges and Solutions in TSV-Based 3D Stacked ICs
16:00 – 23:00	**Social Program**	

Thursday, May, 28

ETS'09
Program At a Glance

9:00 – 10:30	Session 12A Impact of Nanometer Technol. in the Testing Methodology	Session 12B DfT and Embedded Test
10:30 – 11:30	Session 13 - **POSTER III** and Coffee Break	
11:30 – 12:30	Session 14A **Emb. Tutorial 3** Ensuring High Testability without Degrading Security	Session 14B **Emb. Tutorial 4** On-chip Delay Measurem. Tech. for Production Test – from D to A
12:30 – 13:00	Session 15 - **Plenary Closing**	

lunch

Friday, May, 29

ETS'09
Fringe Workshop

9:00 – 13:00 14:30 – 17:00	**Lp on TR** **Impact of Low-Power design on Test and Reliability**

Session 8A

09:00 – 10:30

Advanced Testing of Memories, Power Transistors and Microfluidic Systems

Moderators: *Ondřej NOVÁK, Czech Technical Univ. (Czech Republic)*
Krish CHAKRABARTY, Duke Univ. (USA)

F **Design and Test Challenges in Resistive Switching RAM (ReRAM): An Electrical Model for Defect Injections**
Olivier GINEZ, Jean Michel PORTAL, Christophe MULLER, Univ. de Provence (Aix-Marseille I) (France)

F **Novel Solution for the Built-in Gate Oxide Stress Test of LDMOS in Integrated Circuits for Automotive Applications**
Vezio MALANDRUCCOLO, Mauro CIAPPA, Wolfgang FICHTNER, Swiss Federal Inst. of Technology (ETH) (Switzerland); Hubert ROTHLEITNER, Infineon Technologies (Austria)

F **Built-in Test Solutions for the Electrode Structures in Bio-Fluidic Microsystems**
Quis AL-GAYEM, Hongyuan LIU, Andrew RICHARDSON, Lancaster University (UK)

Session 8B

09:00 – 10:30

Recent Advances in ATPG

Moderators: *Zebo PENG, Linkoping Univ. (Sweden)*
Nicola BOMBIERI , Univ. of Verona (Italy)

F **Increasing Robustness of SAT-based Delay Test Generation using Efficient Dynamic Learning Techniques**
Stephan EGGERSGLUESS, Rolf DRECHSLER, University of Bremen (Germany)

F **Input Cubes with Lingering Synchronization Effects and their Use in Random Sequential Test Generation**
Irith POMERANZ, Purdue University (USA); Sudhakar REDDY, University of Iowa (USA)

F **Automatic Functional Stress Pattern Generation for SoC Reliability Characterization**
Paolo BERNARDI, Matteo SONZA REORDA, Michelangelo GROSSO, Ernesto SANCHEZ, Politecnico di Torino (Italy); R. CAGLIESI, M. GIANCARLINI, ELES Semiconductor Equipment (Italy); Davide APPELLO, STMicroelectronics (Italy)

Q-STAR TEST
The Current Test Company

Innovation
in
Test & Measurement

We offer:
- DFT and Test related consulting and training services
- Advanced current measurement products & solutions
- Engineering services serving design, prototyping & test
- Electronic prognostic solutions.

Enabling:
- Up to 10x Test Time & Cost Reduction
- Test Data and Product Quality Improvement
- Faster Failure Analysis (1 day)
- 0ppm Quality & Reliability at low cost

When Failure is not an option, when quality of engineering, cost reduction, test quality and data quality are keys, visit **www.qstar.be** for more information or contact us to discover the rewards of our solutions.

Q-Star Test: Innovation in Test & Measurement

Alanda Room

Session 8C

09:00 – 10:30

Student´s Forum

Moderators: *John HAYES, Univ. of Michigan (USA)*
Ilia POLIAN, Freiburg Univ. (Germany)

Resistive Bridging Faults-Defect-Oriented Modeling and Efficient Testing
Piet ENGELKE, Albert-Ludwigs-University, Freiburg (Germany)

Power-Supply and Temperature Based Methodologies to Improve Tolerance and Detection of Delay Faults in Synchronous Digital Circuits
Jorge SEMIÃO, IST/INESC-ID, Univ. Algarve (Portugal)

Improving SATbased ATPG
Alejandro CZUTRO, Albert-Ludwigs-University, Freiburg (Germany)

Advanced Techniques for Automatic Test Pattern Generation using Boolean Satisfiability
Daniel TILLE, University of Bremen (Germany)

Fault Tolerance Architecture for Reliable Hybrid CMOS/ Nanodevices Memory
Nor Zaidi HARON, Said HAMDIOUI, Delft University of Technology (The Netherlands)

Current Monitoring of Power Structures Using Magnetic Force Sensor
Martin DONOVAL, Martin DAŘíČEK, Juraj MAREK, Viera STOPJAKOVÁ, Slovak University of Technology (Slovakia)

SoC Yield Improvement for Future Nanoscale Technologies
Julien VIAL, A. Virazel, A. Bosio, L. Dilillo, P. Girard, C. Landrault, S. Pravossoudovitch, LIRMM (France)

Testing of Delay Faults in Asynchronous Circuits
Roland DOBAI, Slovak Academy of Sciences (Slovakia)

Performance/hardware overhead estimation of ADC BIST implementations
Peter MRAK, Jozef Stefan Institute (Ljubljana, Slovenia)

A Mixed HDL/PLI Test Package
Nastaran NEMAT, University of Tehran (Iran)

A Logic Diagnosis Approach for Sequential Circuits
Youssef BENABBOUD, LIRMM and STMicroelectronics (France); A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, LIRMM (France); L. Bouzaida, I. Izaute, STMicroelectronics (France)

Test Pattern Generation and Compaction for Crosstalk Induced Glitch Faults
Shehzad HASAN, University of Bremen (Germany)

Session 9

10:30 – 11:30

Student´s Posters

Session 10A

11:30 – 13:00

Avenida Room

Advanced External Testing of Mixed-Signal Cores

Moderators: *Einar AAS, Norway Univ. of Science (Norway)*
Luz BALADO, Univ. Pol. de Catalunya (Spain)

F **Defect Filter for Alternate RF Test**
Haralampos STRATIGOPOULOS, Salvador MIR, TIMA Laboratory (France); Erkan ACAR, Duke University (USA); Sule OZEV, Arizona State University (USA)

F **Signature-Based Testing for Digitally-Assisted Adaptive Equalizers in High-Speed Serial Links**
Mohamed ABBAS, University of Tokyo (Japan); Kwang-Ting (Tim) CHENG, Univ. of California (Santa Barbara, USA); Yasuo FURUKAWA, ADVANTEST Corp. (Japan); Satoshi KOMATSU, Kunihiro ASADA, University of Tokyo (Japan)

I **Optimization of a Structural DfT Targeting Fault Detection on High-Speed ADCs**
Yolanda LECHUGA, Roman MOZUELOS, Mar MARTINEZ, Salvador BRACHO, Universidad de Cantabria (Santander, Spain)

Remember

F formal

I informal

V vendor

Almenara Room

Session 10B

11:30 – 13:00

Diagnosis and Dependability Analysis

Moderators: *Peter HARROD, ARM, (UK)*
Alex BYSTROV, Newcastle Univ. (UK)

F **A Two Phase Approach for Minimal Diagnostic Test Set Generation**
Mohammed SHUKOOR, Vishwani AGRAWAL, Auburn University (USA)

F **Categorizing and Analysis of Activated Faults in the FlexRay Communication Controller Registers**
Yasser SEDAGHAT, Seyed Ghassem MIREMADI, Sharif University of Technology (Tehran, Iran)

I **Improving Diagnostic Test Generation for Scan Chain Failures Using Multi-Cycle Sequential Patterns**
Xun TANG, Univ. of Iowa (USA); Ruifeng GUO, Wu-Tung CHENG, Mentor Graphics Corp. (USA); Sudhakar REDDY, Univ. of Iowa (USA); Yu HUANG, Mentor Graphics Corp. (USA)

Alanda Room

Session 10C

11:30 – 12:30

Special Session on Soft Errors in Electronic Systems

Moderators: *Sybille HELLEBRAND, Univ. of Paderborn (Germany)*
Raoul VELAZCO, TIMA (France)

Complex Electronic Systems Soft Error Rate (SER) Management
Dan Alexandrescu, Iroc (France); Shi-Jie Wen, Cisco (USA); Michel Nicolaidis, TIMA Lab. (France)

Abstract : This talk describes recent breakthroughs on Single Event Effects analysis techniques for complex ASICs and SoCs. We propose a systematic method for the evaluation of the system Soft Error Rate (SER) based on reliability-like, higher-level SER budgeting and hierarchical breakdown of SER constraints through all the levels of the design flow from the system architecture to the final chip implementation. The approach is particularly adapted for evaluating the SER of difficult-to-tackle sophisticated SoCs, such as networking chips, whose designers are confronted today with increasingly demanding reliability requirements. Practical mitigation solutions guided from the analysis results are also addressed.

Session 11A

14:30 – 15:30

Embedded Tutorial 1

Moderator: *Bernd BECKER, Freiburg University (Germany)*

Switching Noise and Process Variability Challenges in Delay Testing

Adit SINGH, Auburn University (USA)

Abstract : Delay defects that degrade performance and cause reliability failures are emerging as a major problem in nanometer technologies. Small delay defects represent a significant reliability concern when resistive defects are present in a technology. A low level of resistive defects can be overcome with typical TDF testing, however when the defect rate increases, traditional TDF testing is insufficient to achieve low DPPM levels. Today, additional stresses are necessary to age these defects to the point where TDF tests can screen them. In order to achieve low DPPM levels without additional acceleration such as burn-in, fine delay defect screening appears to offer a solution. Structural scan based delay testing is being actively pursued as a possible solution. However, recent research indicates that several formidable challenges must be overcome before it can become fully effective. A major limitation of scan timing tests is that they operate the circuit outside of the normal functional mode. The single fast launch-tocapture clock period in the scan test is assumed to provide a single cycle snapshot of circuit timing observed in uninterrupted normal functional operation. Signal delays in this clock window are checked and verified against the desired clock rate.

Unfortunately, this observed signal timing may not reflect true circuit delays in normal functional operation for several reasons. (1) Power supply noise (IR drops) from abnormal excessive switching activity from scan vectors. (2) Activation of multi-cycle paths and false paths. (3) Excessive coupling noise and crosstalk effects due to non-functional switching patterns. (4) Device performance variation due to a different die temperature profile during test as compared to functional operation. (5) “Clock stretching” -the inability of the clock tree to reach timing stability for a single fast capture clock pulse. It is to avoid unacceptable yield loss from false failure indications (“over testing”) due to these timing uncertainties that force scan delay tests to be often run slower than rated speed, limiting their effectiveness. Detection of small delay defects by scan tests is further compromised by additional factors that also impact functional timing tests: (6) Timing margins required to allow for the increasing variations in process parameters. (7) Short paths that can absorb many small delay defects within the circuit timing slacks.

The proposed tutorial will explain and illustrate these test challenges. State-of-the-art test methodologies aimed at overcoming these challenges are presented, and their effectiveness and limitations discussed, based on published experimental studies. These include using only functionally validated LOC test vectors to mimic (one-cycle) functional operation during the scan test thereby avoiding abnormal circuit activity and activation of false paths; multi-cycle capture to minimize clock stretching as supported by EDA test tools; Cadence’s Tru-Time based faster-thanratedclock test methodology to target small delay defects on short paths; and Scan delay test based speed binning studies from Nvidia and Freescale. Promising new research ideas not yet adopted by industry, such as comparison timing testing of multi-core processors, will also be discussed.

Session 11B

14:30 – 15:30

Embedded Tutorial 2

Moderator: *Yervant ZORIAN, VirageLogic (USA)*

Test Challenges and Solutions in TSV-Based 3D Stacked ICs

Krishnendu CHAKRABARTY, Duke University (USA)
Erik Jan MARINISSEN, IMEC (Belgium)

Abstract : In the continuing quest for high-density high-performance low-power integrated circuits, new developments in processing technology now start to allow us to stack multiple integrated circuits on top of each other, interconnected by many Through-Silicon Vias (TSVs). This next step in the sequence flipchip, Multi-Chip Module, and System-In-Package, has multiple attractive benefits: (1) Heterogeneous integration: each die can be made in a dedicated technology, for example optimized for digital logic, memory, analog, RF, sensors, etc.; (2) Higher yield, if one large die is divided over multiple smaller dies; (3) Small footprint, as multiple dies are stacked vertically on top of each other; (4) Small volume, as dies are thinned and stacked with very little space in between; (5) High performance, as TSVs allow much faster and wider communication paths between dies than traditional wires; and (6) Low power, as TSVs have much less capacity than traditional wires.
While architects, designers, and EDA folks are preparing to take advantage of the new third dimension in chip design, test solutions should follow suit in order to make this technology industrially viable.
This embedded tutorial gives an overview of the field and highlights the corresponding test challenges and emerging test solutions. It targets both industrial engineers, who want to be prepared for what is ahead, as well as researchers that hope to contribute to this hot and exciting domain.

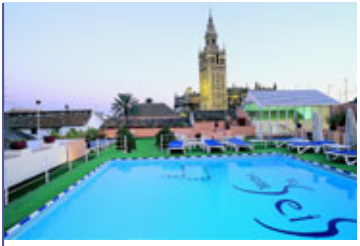
Social Program

16:00 – 23:00

The social event will consist of two parts: **A sightseeing tour and the Gala Dinner**.

The touring part includes visiting two of the most beautiful and historic landmarks in Seville: the *Mudejar Royal Palace*, known as *Reales Alcázares*, and the *Casa de Pilatos* (*Pilate's House*), followed by a walk around the old-town Jewish quarter, named *Barrio de Santa Cruz*.

Divided into groups, the buses will bring us directly to the *Casa de Pilatos*. After visiting it, every group will make a short guided walk, including a refreshing drink stop, through some of the most interesting alleys of the *Barrio de Santa Cruz* , before heading for the *Reales Alcázares*.



After the visit, all groups will meet for the Gala Dinner at the Restaurant located at the Hotel Los Seises, which is situated off the Cathedral, at the rear of the archbishop's palace. This sixteenth-century building was recently converted in a hotel, where pieces from different artistic ages are on display. There, Roman mosaics and thermals go hand in hand with avant-garde furniture. Renaissance panelling coexists with arabic tiling, paving and columns. The building is crowned by a terrace with a swimming pool, an ideal observatory to have a night glimpse to the nearby Cathedral and the majestic Giralda tower.

www.hotellosseises.com

The Palace known as the Casa de Pilatos, was chiefly built between the 15th and 16th centuries, and springs from the union of the Enríquez and Ribera families. Located in the historical part of Seville's city centre, this palace is a delicate combination of late-medieval Gothic and Mudejar tradition and the innovations of the Renaissance. The successive purchases of houses and sites by the Enríquez de Ribera family resulted in the gradual addition of drawing rooms, courtyards and gardens, leading it to became the biggest private residence in Seville.

www.fundacionmedinaceli.org/monumentos/pilatos/

The construction of the Mudejar Royal Palace (Reales Alcázares) was ordered by Abd Al-Rahman III, the first Caliph of Andalusia, in the year 913, over an ancient Roman and Visigoth settlement. Many additions was made by The King Pedro I, known as The Cruel, during years 1364-1366. Actually is one of the most important examples of Mudéjar architecture in Sevilla

www.patronato-alcazarsevilla.es

Almenara Room

Session 12A

09:00 – 10:30

Impact of Nanometer Technologies in the Testing Methodology

Moderators: *Michel RENOVELL, LIRMM (France)*
Salvador MANICH, Univ. Pol. de Catalunya, Spain

F **Low-Complex Off-Chip Skew Measurement and Compensation Module (SMCM) Design for Built-Off Test Chip**
Kihyuk HAN, Joonsung PARK, Jae Wook LEE, Jacob ABRAHAM, The Univ. of Texas at Austin (USA); Eonjo BYUN, Cheol-Jong WOO, Sejang OH, Samsung Electronics (Korea)

I **New Repeatability & Reproducibility Methodology for Semiconductor Testing**
Sergio TENUCCI, Marco SPINETTA, Alberto PAGANI, Bernard RANCHOUX, STMicroelectronics (Italy and France)

F **A voltage-mode testing method to detect IDDQ defects in digital circuits**
Josep RIUS, Univ. Pol. Catalunya (Spain); Luis ELVIRA, Maurice MEIJER, NXP Semiconductors (The Netherlands)

Session 12B

09:00 – 10:30

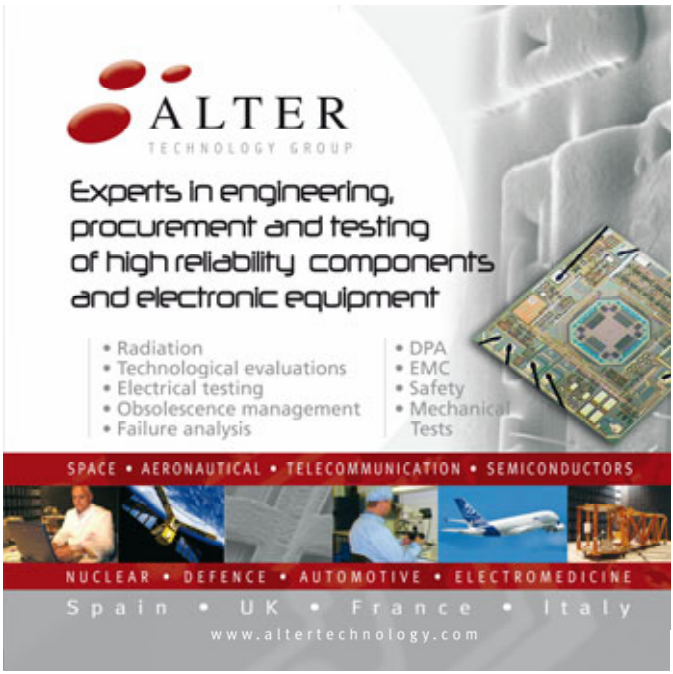
DfT and Embedded Test

Moderators: *Jerzy TYSZER, Poznan Univ. of Technology (Poland)*
Andreas GLOWATZ , Mentor Graphics Hamburg (Germany)

F **Partial Scan Approach for Secret Information Protection**
Michiko INOUE, Tomokazu YONEDA, Muneo HASEGAWA, Hideo FUJIWARA, Nara Institute of Science and Technology NAIST (Japan)

F **Masking of X-values by use of a hierarchically configurable register**
Thomas RABENALT, Univ. of Potsdam, Andreas LEININGER, Infineon Technologies AG, Michael GOESSEL, Univ. of Potsdam (Germany)

F **Test Encoding for Extreme Response Compaction**
Stefan HOLST, Michael KOCHTE, Melanie ELM, Hans-Joachim WUNDERLICH, Univ. of Stuttgart (Germany)



Session 13

10:30 – 11:30

Poster Session III

Memory Test and Diagnosis using Automated Pattern Generation
Joerg VOLLRATH, Qimonda AG (Germany)

Test Data Reduction by Test Point Insertion Based on Necessary Assignment
Kazuko HIRAMOTO, Yuki YOSHIKAWA, Hideyuki ICHIHARA, Tomoo INOUE, Hiroshima City University (Japan)

Start-Up of a Pulsed Laser Test System for Single Event Effects Analysis
Fco. Rogelio PALOMO PINTO, Juan MOGOLLÓN, Javier NÁPOLES, Hipólito GUZMÁN MIRANDA, José RODRíGUEZ, Alfredo VEGA-LEAL, Miguel AGUIRRE, J. TOMBS, Univ. of Sevilla; C. MÉNDEZ, J. R. VÁZQUEZ DE ALDANA, P. MORENO, Univ. of Salamanca, L. ROSO, Centro de Láseres Pulsados Ultracortos Ultraintensos CLPU, Salamanca (Spain)

Improving Soft Error Correction Capability of 4-D Parity Codes
Muhammad IMRAN, Zaid AL-ARS, Georgi GAYDADJIEV, Delft University of Technology (The Netherlands)

Handling More X's Using Current X-Tolerant Compactors with Maximal Compaction
Youhua SHI, Nozomu TOGAWA, Masao YANAGISAWA, Tatsuo OHTSUKI, Waseda University (Japan)

A Black-Box Software-Based Self-Test for Embedded Microprocessors
Stefano di CARLO, Paolo PRINETTO, Gianfranco POLITANO, Alessandro SAVINO, Politecnico di Torino (Italy)

Fast BER Test for Digital RF Transceivers
Jerzy DABROWSKI, Linkoping Univ. (Sweden)

A BiST Jitter Characterization Solution for use with Low Cost Automatic Test Equipment
Sachin DASNURKAR, Jacob ABRAHAM, The Univ. of Texas at Austin (USA)

Session 14A

11:30 – 12:30

Embedded Tutorial 3

Moderator: *Adelio SALSANO, University of Roma II (Italy)*

Ensuring High Testability without Degrading Security

Giorgio di NATALE, Marie-Lise FLOTTES, Bruno ROUZEYRE, LIRMM (France)
Paolo MAISTRI, Regis LEVEUGLE, TIMA Lab. (France)

Abstract : Cryptographic algorithms are used to protect sensitive information from untrusted parties when the communication medium is not secure. Many secure systems such as smartcards include hardware implementation of symmetric cryptographic algorithms such as (Triple) Data Encryption Standard and Advanced Encryption Standard. The secret keys used to encrypt the data with these algorithms are large enough to prevent any brute force attack that consists in exploring the whole solution space. However, the hardware implementation of these cryptographic algorithms allows the hackers to measure the observable characteristics of the physical implementation and deduce the secret key (side-channel attacks). The key can even be discovered by applying a side-channel attack on scan chains. These scan chains, which aim to provide full controllability and observability of internal states, represent nevertheless the most popular design-for-testability scheme. Because crypto-processors and others cores in a secure system must pass through high-quality test procedures to ensure that data are correctly processed, testing of crypto chips faces a dilemma: how to develop a design-for-testability scheme that provides high testability (high controllability and observability) while maintaining high security (minimal controllability and observability)? This tutorial presents the security weaknesses generated by scan designs on hardware AES and DES implementations. It also discusses the pros and cons of security-dedicated DFT, BIST and Fault tolerance solutions taken from the literature.

IEEE
Celebrating 125 Years
of Engineering the Future

Avenida Room

Session 14B

11:30 – 12:30

Embedded Tutorial 4

Moderator: *Hans KERKHOFF, Univ. Twente (The Netherlands)*

On-chip Delay Measurement Techniques for Production Test – from Digital to Analog

Stephen SUNTER, LogicVision (USA)

Abstract : As CMOS IC dimensions scale below 90 nm, delays-of-interest range from nanoseconds to picoseconds. Greater time measurement accuracy is needed but off-chip delay measurement techniques are becoming severely limited by fundamental properties of signal access paths off-chip and on-chip, such as noise, wire length, and impedance variation. On-chip measurement techniques have been proposed by IC designers, DFT engineers, and test engineers, with claimed accuracies ranging from nanoseconds to femtoseconds, at least in simulation.

This embedded tutorial will survey most of the papers that provide silicon results published in the last 10 years, in both design and test journals/ conferences, and some representative papers that include only simulated results, to discover the most promising directions for measuring and production testing today's and future delays-of-interest. Delay parameters include instantaneous delay, average delay, and delay variation (long and short term, including jitter) in digital and analog paths, which inevitably depend on voltage, frequency, and temperature. The measurement techniques will be categorized by suitability for measurement of one-shot and periodic events, then by measurement principle, and lastly by circuit technique and reported real-silicon capabilities. The goal is to identify principles and general techniques suitable for production testing of digital and perhaps analog circuitry, which means high resolution, wide range, quick test time, process tolerance, and insignificant silicon area.

Avenida Room

Closing Session

12:30 – 13:00

Closing Remarks 12:30 – 12:45

Jose Luis HUERTAS, IMSE-CNM (Spain) - ETS'09 General Chair

Introduction to ETS´10 12:45 – 13:00

Ondřej NOVAK, Czech Technical Univ. (Czech Republic) - ETS'10 General Chair

ETS´09 Fringe Workshop

09:00 – 13:00 and 14:30 – 17:30

Chair: *Alex Bystrov, Newcastle University (UK)*
Co-Chair: *Patrick Girard, LIRMM (France)*

2nd International Workshop on Impact of Low-Power Design on Test and Reliability (LPonTR'09)

The LPonTR workshop aims to bring together design, reliability and test engineers and researchers to discuss the impact of advanced low-power / low voltage design methodologies of nanometer silicon systems on test and reliability. Power and thermal issues, leakage, process variations, enhanced susceptibility to environmental and operation-induced disturbances are physical constraints that drive the need to the development of low-power, process-tolerant design techniques. However, these techniques generate a new set of test and reliability challenges, questing for an innovative set of methodologies and tools.

14th European Test Symposium

NH Central Convenciones Hotel

Sevilla, Spain

May 25-29, 2009

Notes


ALTER
TECHNOLOGY GROUP SPAIN


ARM


Mentor
Graphics


OPTIMAL
TEST
MASTERING TEST MANAGEMENT


Q-STAR
TEST
The Current Test Company


SYNOPSYS


testinsight
www.testinsight.com

Instituto de Microelectrónica de Sevilla
www.imse-cnm.csic.es