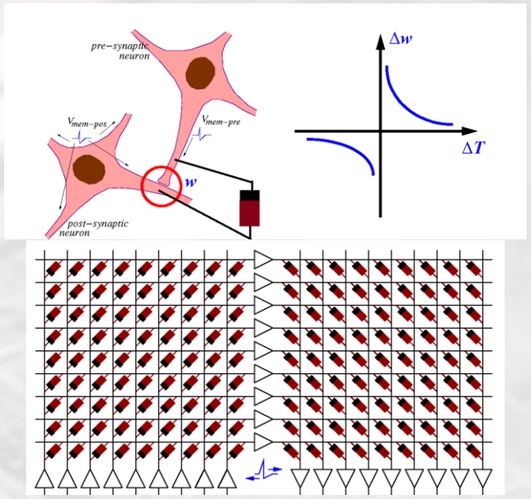

EU Projects

NABAB: Nano Computing Building Blocks with Acquired Behaviour. FP7-216777

CAVIAR: Convolution Address-Event-Representation (AER) Vision Architecture for Real-Time. FP5-IST-2001-34124

PNEUMA Plasticity in Neural Memristive Architectures. PRI-PIMCHI-2011-0768.

NEURAM3: NEUral computing aRchitectures in Advanced Monolithic 3D-VLSI nano-technologies. H2020: ICT 25-2015-687299

HBP: The Human Brain Project. H2020-HBP-604102

ECOMODE: Event-driven compressive vision for multimodal interaction with mobile devices. H2020-ICT-2014-1-644096

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Neuromorphic Systems Group

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University of Seville - US

Since its coordination of the EU CAVIAR project (www.imse-cnm.csic.es/caviar), the IMSE Neuromorphic group develops sensory and processing microchips that mimic sensing and processing in biological beings. It also develops multi-chip and hybrid chip-FPGA systems to scale up to higher complexity systems. The group also works on algorithms and sensory processing for spiking information sensing, coding and processing. Chips use mixed signal, low current, and/or low power, circuit techniques, as well as high speed communication techniques. The group uses mixed or digital CMOS technologies, as well as application projections exploiting emergent nanoscale technologies or new devices like memristors

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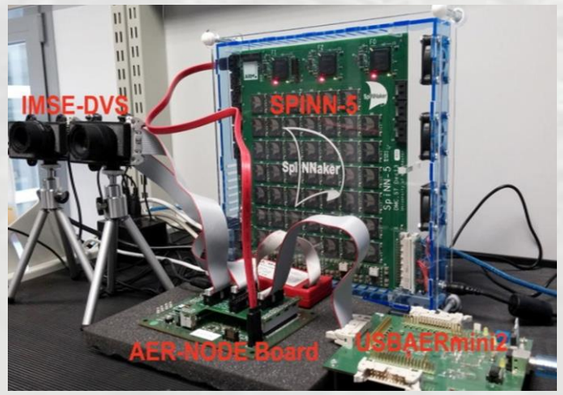
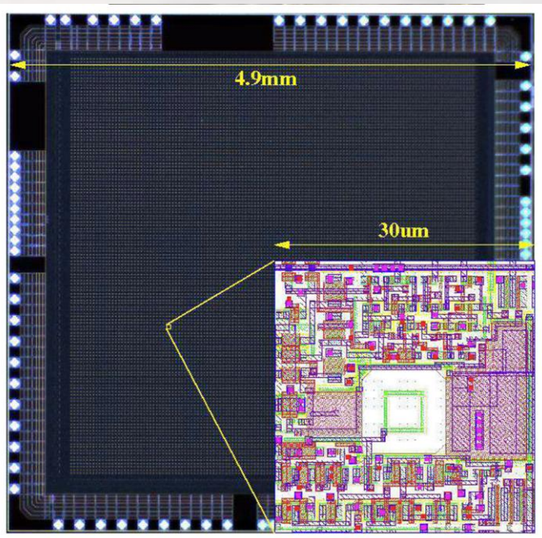
Research Lines:

- ✓ Bioinspired Vision Sensors
- ✓ Spiking Convolution Chips
- ✓ Multi-chip and Hybrid Chip-FPGA processors
- ✓ Sensory-Processing on the SpiNnaker platform
- ✓ Spiking Information Processing
- ✓ Spike Learning
- ✓ Low-power, low-current circuits
- ✓ High-speed communication
- ✓ Neuromorphic systems with memristors





Bioinspired Vision Sensors

Event-driven retinas do not produce sequences of still frames, as conventional video cameras do. Instead, each pixel senses light and computes a given property (spatial contrast, temporal change) continuously in time. Whenever this property exceeds a given threshold, the pixel sends out a spike coded as an address event (which usually consists of the pixel x,y coordinate and the sign of the threshold), which is written onto one (or more) high speed bus with asynchronous handshaking. This way, sensors produce continuous event flows, and subsequent processors process them event by event.

The group has developed a catalog of spiking vision sensors:

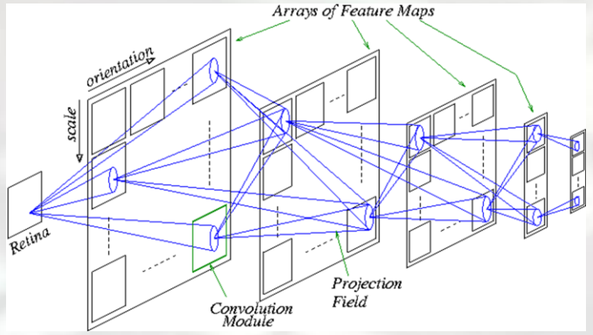
- ✓ 128x128 Temporal Contrast Retina with Improved Contrast Sensitivity and Reduced FPN (Serrano 2013)
- ✓ 128x128 Temporal Contrast Retina with Improved Contrast Sensitivity (Leñero 2011)
- ✓ 32x32 Spatial Contrast Retina with On-chip Calibration and Time-to-first Spike Mode (Leñero 2010)
- ✓ 32x32 Spatial Contrast Retina with On-chip Calibration (Costas-Santos 2007)

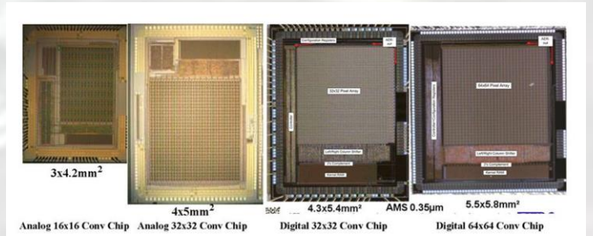
Spiking ConvNets

Convolutional Neural Networks (ConvNets) are bioinspired hierarchical architectures that perform complex recognition tasks. They are commonly used in deep networks artificial intelligence vision systems. However, they do computation and object recognition on still frames. The connection weights are trained using conventional backpropagation algorithms on sets of static training images. The IMSE Neuromorphic group has done research on algorithms and hardware for implementing third generation spiking neural networks using spiking ConvNets.

They have a catalog on fully programmable weights and modularly interconnectable Spiking Convolution microchips:

- ✓ 64x64 AER Convolution Chip with Digital Pixel Operation, Multikernel Capability, Kernels with up to 32x32 weights, and 175ns latency. (Camuñas 2012)
- ✓ 32x32 AER Convolution Chip with Digital Pixel Operation, Kernel up to 32x32 weights, and 155ns latency. (Camuñas 2011)





- ✓ 32x32 AER Convolution Chip with Analog Pixel Operation and Kernel up to 32x32 weights (Serrano 2006)
- ✓ 16x16 AER Convolution Chip with Analog Pixel Operation Kernel up to 16x16 weights (Serrano 2008)

The group has also developed programmable modular Spiking ConvNets using routers and convolutional modules implemented on FPGAs

- ✓ Reconfigurable 2D array of AER Convolution Processors on a Virtex6 FPGA (Zamarreño 2013, Camuñas18).
- ✓ Node Board: special purpose board to be modularly assembled in a 2-D grid fashion to build large scale spiking convolution networks. Each node contains a 2-D grid of convolution modules inside the same FPGA XC6SLX150T Spartan6 and four SATA connectors to assemble the boards in a 2D-mesh fashion. Additionally, the board contains two parallel AER connectors to link the FPGA with external AER components (AER sensors, AER convolution chips, etc…)

Memristive NCSs

The group has proposed and designed Neuromorphic Computing Systems (NCSs) based on hybrid combination of CMOS spiking neurons and dense memristive synaptic arrays. The memristor devices when stimulated with different waveforms of pre and post spikes undergo a variety of bioinspired Spike-Time-Dependent-Plasticity (STDP) rules . (Serrano2013b). Memristive NCS are promising canditates to implement very large scale low power self-learning systems.