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F. Medeiro, R. del Río, B. Pérez-Verdú and A. Rodríguez-Vázquez

Instituto de Microelectrónica de Sevilla - Centro Nacional de Microelectrónica  
Avda. Reina Mercedes s/n, (Edif. CICA)  
E-41012, Sevilla, Spain

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# Practical considerations for the design of cascade multi-bit high-frequency $\Sigma\Delta$ modulators

F. Medeiro, R. del Río, B. Pérez-Verdú and A. Rodríguez-Vázquez

Instituto de Microelectrónica de Sevilla - CSIC  
Edificio CICA-CNM, C/Tarfia sn, 41012-Sevilla, SPAIN  
Phone #34 5 4239923, FAX #34 5 4231832, e-mail: medeiro@imse.cnm.es

## Abstract

Recommendations are given for efficient design of high-frequency  $\Sigma\Delta$  modulators using multi-stage (cascade) multi-bit quantization architectures. These cover from pure architectural aspects to cell design with special emphasis on the impact of circuit imperfections. Conclusions are validated by measurements on a 13-bit 2.2MS/s prototype fabricated in a 0.7 $\mu$ m CMOS technology.

## 1. Introduction

Nowadays, several industrial applications have renewed the interest on extending the use of  $\Sigma\Delta$  modulators ( $\Sigma\Delta$ 's) up to the communication range and above [1]. In fact, using oversampling and noise-shaping techniques for high-performance A/D conversion is becoming more and more attractive as poor-analog-performance technologies are imposed. However, because the signal bandwidth  $f_x$  and the sampling frequency  $f_s$  of a  $\Sigma\Delta$  converter are related through the oversampling ratio  $M = f_s/(2f_x)$ , increasing the signal frequency while keeping achievable sampling frequency and low-power consumption implies a reduction of  $M$  required to obtain given resolution. This last can be estimated, considering only quantization error, as follows:

$$B(\text{bit}) = \frac{1}{2} \log_2 [(2^b - 1)^2 (2L + 1) M^{2L+1} / (\pi^{2L})] \quad (1)$$

where  $b$  is the resolution (bit) of the internal quantizer and  $L$  is the modulator order. It is clear from (1) that high-order multi-bit quantization  $\Sigma\Delta$ 's are natural candidates to achieve high-resolution, high-speed A/D conversion. However two important drawbacks arise: on the one hand, unlike 1st- and 2nd-order loops, high-order loops are not unconditionally stable; on the other, the linearity of a multi-bit  $\Sigma\Delta$  is ultimately limited by that of the multi-bit DAC in the feedback path. Among the solutions found in literature [2], there is one in great accordance with the  $\Sigma\Delta$  principles because it does not need any correction mechanism. The basic idea consists of: first, performing the high-order filtering by cascading low-order (1st- and 2nd-)  $\Sigma\Delta$ 's [3] to guarantee unconditional stability; and, second, using multi-bit quantization only at the last stage of the cascade to attenuate the influence of the multi-bit DAC non-linearity [4].

This paper focuses on such  $\Sigma\Delta$ 's, giving practical reci-

pes for their successful integration in sub-micron CMOS technologies. Architectural issues are covered in Section 2. Section 3 is devoted to the impact of circuit imperfections. In Section 4, our conclusions are validated through the measurements of a 13-bit, 2.2MS/s  $\Sigma\Delta$  for ADSL in 0.7 $\mu$ m CMOS.

## 2. Architectural aspects

Fig.1 shows a generic  $L$ th-order  $N$ -stage multi-bit  $\Sigma\Delta$ . After digital cancellation of the low-order quantization errors, the following is obtained for the Z-domain output,

$$Y = z^{-L}X + d(1 - z^{-1})^L E_N - d(1 - z^{-1})^{(L-L_N)} E_D \quad (2)$$

where  $X$  is the Z-transform of the modulator input,  $d$  is an scalar larger than unity to compensate for signal scaling in the cascade,  $E_N$  is the last-stage quantization error, and  $E_D$  is the error induced in the last stage DAC. Note that  $E_D$  is  $(L - L_N)$ th-order shaped, which may significantly relax the DAC linearity specification with no correction nor calibration required.

Several cascade multi-bit architectures have been proposed: (a) 3rd-order 2-stage cascade (2-1mb) [4], (b) 4th-order 2-stage cascade (2-2mb) [5] and (c) 4th-order 3-stage cascade (2-1-1mb) [6]. According to (2), DAC-induced error is 2nd-order shaped in the first two modulators and 3rd-order shaped in the last one. Thus, while in the 2-1mb and 2-2mb architectures the in-band power of such error is attenuated by  $M^5$ , in the 2-1-1mb it is attenuated by  $M^7$ . This reduces the sensitivity of the latter to the non-linearity so that DAC INL as large as 1%FS does not significantly degrade the performance of the 2-1-1mb modulator. We will center on this architecture whose block diagram is shown in Fig.2. The cancellation logic

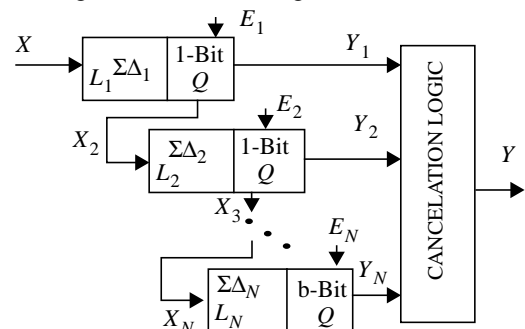


Fig. 1. Generic  $L$ th-order  $N$ -stage cascade multi-bit  $\Sigma\Delta$

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is also shown. The transfer function of the digital blocks and the relationships among digital and analog coefficients required to correctly cancel the low-order single-bit quantization error are given in Table 1. With this, (2) turns

$$Y = z^{-4}X + d_3(1 - z^{-1})^4 E_3 - d_3(1 - z^{-1})^3 E_D \quad (3)$$

and the in-band error power is

$$P_{2-1^2 mb} \cong d_3^2 \left( \sigma_Q^2 \frac{\pi^8}{9M^9} + \sigma_D^2 \frac{\pi^6}{7M^7} \right) \quad (4)$$

where

$$\begin{aligned} \sigma_Q^2 &\cong [\Delta / (2^b - 1)]^2 / 12 \\ \sigma_D^2 &\cong \frac{1}{2} \Delta^2 \left( \frac{INL}{100} \right)^2 \end{aligned} \quad (5)$$

are the quantization and DAC-induced error powers, respectively, with *INL* expressed in %FS.

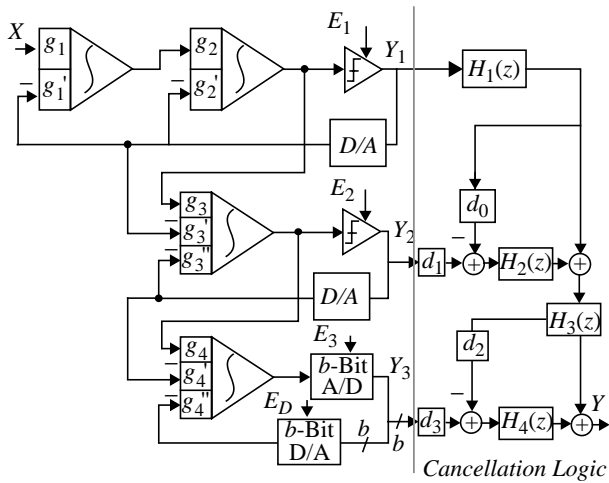
**Table 1.** Digital blocks and coefficient relations in Fig.2

Digital	Digital/Analog	Analog
$H_1(z) = z^{-1}$	$d_0 = 1 - \frac{g_3'}{g_1 g_2 g_3}$	$g_1' = g_1$
$H_2(z) = (1 - z^{-1})^2$	$d_1 = \frac{g_3''}{g_1 g_2 g_3}$	$g_2' = 2g_1' g_2$
$H_3(z) = z^{-1}$	$d_2 = 0$	$g_4' = g_3'' g_4$
$H_4(z) = (1 - z^{-1})^3$	$d_3 = \frac{g_4''}{g_1 g_2 g_3 g_4}$	

### 2.1 Selection of analog coefficients

Apart from the relationships of Table 1, a proper selection of the analog and digital coefficients should take into account the following considerations:

- Overloading of modulator-stages should be avoided by properly scaling the signals transferred among them.
- The output swing needed in the integrators must be



**Fig. 2.** 4th-order 3-stage 2-1-1 cascade multi-bit  $\Sigma\Delta M$

physically achievable. In particular, using a small weight for the first integrator is highly recommended because it reduces the amplifier output swing and slew-rate requirements.

- Digital coefficient  $d_3$  which amplify the last-stage quantization error in (4), should be as small as possible.

Additional considerations in order to simplify the implementation are:

- The digital coefficients should be 0,  $\pm 1$  or multiple of 2, thus enabling the use of simple right shifters.
- The gain of the multi-bit quantizer, which is imposed by the fact that the last-stage loop gain equals unity, should not be too large.
- Minimize the number of branches required for each integrator and the total number of unitary capacitors.

Several sets of coefficients fulfilling previous requirements have been reported for the architecture considered [6][7] and for its single-bit counterpart [8][9]. These are listed in Table 2.

**Table 2.** Coefficients in Fig.2.

	[6]	[8]*	[9]*	[7]
$g_1, g_1'$	0.25	1/3	0.5	0.25
$g_2$	0.5	0.6	0.5	1
$g_2'$	0.25	0.4	0.5	0.5
$g_3$	1	5/6	1	1
$g_3'$	0.375	0.5	0.75	0.5
$g_3''$	0.25	1/3	0.5	0.5
$g_4$	4	3	2	2
$g_4'$	1	1	1	1
$g_4''$	1	1	1	1
$d_0, d_1, d_2, d_3$	-2,2,0,2	-2,2,0,2	-2,2,0,2	-1,2,0,2
Total output swing	$2V_r$	$2.4V_r$	$3.5V_r$	$2V_r$
Output current	$I_o$	$1.2I_o$	$2I_o$	$I_o$
3-branch int. needed?	Yes (3rd,4th)	Yes (4th)	Yes (3rd)	No
Unitary capacitors	33	27	18	18

\*. Adapted for multi-bit quantization in the last stage

Choices in [6] and [7] use an small weight for the first integrator so that the total output swing needed in integrators is around twice the reference voltage ( $V_r$ ). The swing is slightly larger for the choice in [8] ( $2.4V_r$ ) and approximately  $3.5V_r$  for [9]. Note that the same scaling should apply for the maximum output current in the first-stage opamps in order to avoid an excessively non-linear settling. Digital coefficient  $d_3$  is 2 in all cases which represents a loss of only **one** bit with respect to the resolution theoretically achievable (1). Coefficients in the fourth column of Table 2 have additional advantages: first, no 3-branch integrators are required and, secondly, as in [9],

the total number of unitary capacitors is 18, considerably smaller than that needed to implement the coefficients in [6] and [8], 33 and 27, respectively.

### 3. Circuit imperfections

Circuit non-idealities degrading the performance of  $\Sigma\Delta$ 's can be grouped in two categories: (a) those that change the quantization noise transfer function, whose effect strongly depends on the architecture considered, for instance integrator leakage and weight mismatching, and (b) those that can be modeled as an error source at the first integrator; such approximation is justified by the fact that the contributions of remaining integrators are attenuated by increasing powers of the oversampling ratio. This is the case of defective settling in integrators, thermal noise, etc. Both categories are considered separately next.

#### 3.1 Integrator leakage and weight mismatch

In practice, mismatching affects the integrator weights so that the relationships in Table 1 are not fulfilled. Furthermore, finite opamp DC-gain induces leakage in integrators. Both non-ideal aspects result in incomplete cancellation of the quantization error generated in the single-bit stages thus degrading the signal-to-noise ratio. Analysis shows that the extra in-band error power due to these non-idealities is:

$$P_E \cong \sigma_C^2 \left[ \frac{(g_1 + g_2 + g_2')^2}{A_V^2} \frac{\pi^2}{3M^3} + 24\sigma_{cr}^2 \frac{\pi^4}{5M^5} \right] \quad (6)$$

where  $\sigma_C^2 \cong \Delta^2/12$  is the quantization error power of a single-bit quantizer,  $A_V$  stands for the integrator DC-gain and  $\sigma_{cr}$  is the standard deviation on capacitor ratios. Typical values of  $\sigma_{cr}$ , which depends on the technology, layout and unitary capacitor, are between 0.1% and 0.2%. Note that eventually this extra noise can mask that in (4), so that there is a practical upper limit for the resolution of the multi-bit quantizer. This limit is evaluated in Fig.3 (thick solid line), which shows the effective resolution of the modulator considered as a function of the last-stage quantizer resolution for several oversampling ratios (depicted over each curve). Shaded region corresponds to typical resolutions needed in communication systems. Note that all curves saturate for a certain value of the last-quantizer resolution. In practice, using multi-bit quantizers on the right side of the limit may be useless.

#### 3.2 Other circuit imperfections

Main error mechanisms belonging to the second category are thermal noise and defective settling error. The in-band power of the former can be estimated as follows:

$$P_{Th} \cong \frac{kT}{4MC_s} + \frac{kT}{2M(C_s + C_p)} \left( \frac{1}{3} + g_m R_{on} \right) \quad (7)$$

where  $k$  is the Boltzman constant,  $T$  is the absolute temperature,  $g_m$  is the opamp transconductance,  $R_{on}$  is the switch on resistance and  $C_s$  and  $C_p$  are the sampling and

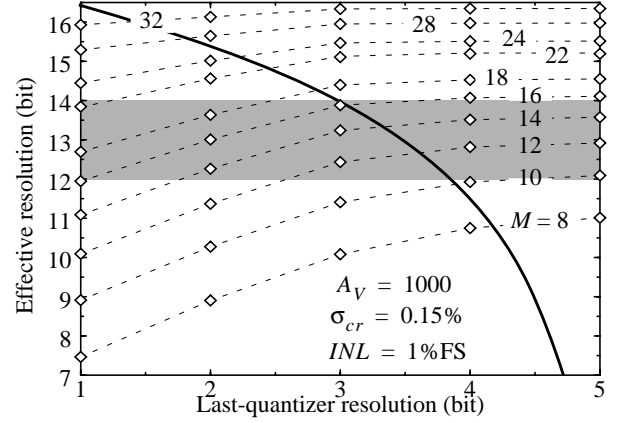


Fig. 3. Achievable modulator resolution vs. last-quantizer resolution for oversampling ratio in the range [8,32].

opamp input parasitic capacitors, respectively. For example, if  $C_s = 0.5$  pF,  $C_p \sim 1$  pF,  $g_m R_{on} \sim 1$ ,  $P_{Th} = -96$  dB which can be clearly neglected for resolutions below 14bit.

More carefully considered should be the defective settling error, whose impact on high-frequency modulator performance is clear. For linear settling (that is, no slew-rate), such error translates into a non-shaped, nearly white noise at the modulator output. It has two main contributions corresponding to the sampling and integration phase errors (see Fig.4), whose in-band powers can be estimated as

$$P_{St_1} \cong \frac{\Delta^2}{9M} \left( 1 + \frac{C_p}{C_o} \right)^2 \left( \frac{C_{l_1}}{C_{eq,1}} \right)^2 \exp\left(-\frac{g_m}{C_{eq,1} f_s}\right) \quad (8)$$

$$P_{St_2} \cong \frac{\Delta^2}{9M} \left( 1 + \frac{C_p}{C_s} \right)^2 \left( \frac{C_s}{C_{eq,2}} \right)^2 \left( 1 + \frac{C_{l_2}}{C_o} \right)^2 \exp\left(-\frac{g_m}{C_{eq,2} f_s}\right)$$

respectively, where  $C_o$  is the integration capacitor and

$$C_{eq,1} = C_p + C_{l_1} (1 + C_p/C_o) \quad (9)$$

$$C_{eq,2} = C_s + C_p + C_{l_2} [1 + (C_s + C_p)/C_o]$$

stand for the opamp equivalent load during sampling and integration phase, respectively.  $C_{l_1}$  and  $C_{l_2}$  are the integrator loads during both phases. Note that they can be rather different because while  $C_{l_2}$  is formed by the parasitic at the integrator output node (partially due to the bottom-plate parasitic of  $C_o$ ),  $C_{l_1}$  is, in addition, the summation of the next integrator sampling capacitors. For non-linear settling, previous expressions remain valid if the maximum opamp output current fulfills the following relation,

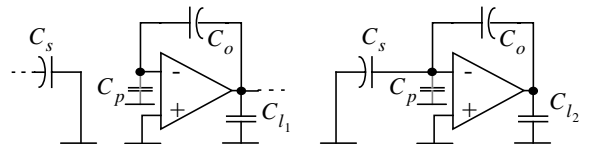
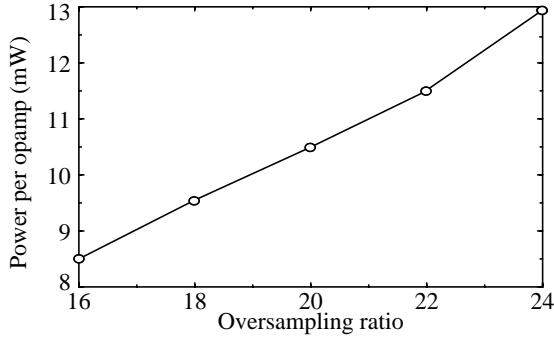


Fig. 4. SC integrator configurations: (a) sampling phase, (b) integration phase.



**Fig. 5.** Estimated power per opamp vs. oversampling ratio

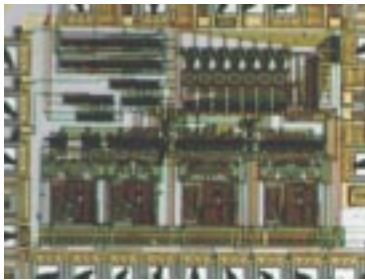
$$I_o = g_m^*(C_s/C_{eq,2})(1 + C_{l2}/C_o)(\Delta/4) \quad (10)$$

where  $g_m^*$  is the opamp transconductance needed to make the settling error power  $P_{Sr} = P_{Sr1} + P_{Sr2}$  in (8) negligible with respect to quantization error power, (4)+(6).

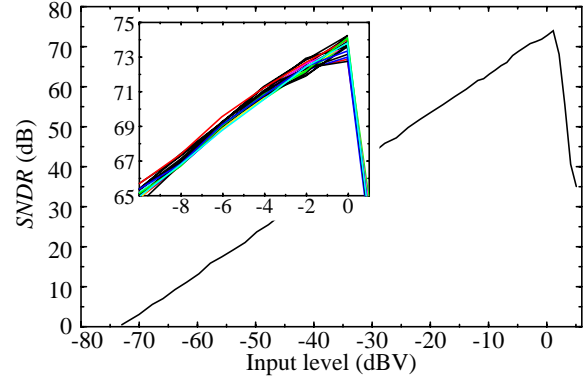
Fig.5 shows the estimated power per opamp needed not to degrade the modulator resolution (with respect to that in Fig.3) as a function of the oversampling ratio, for 2.2MS/s Nyquist rate. Estimation has been made considering single-stage fully-differential folded-cascode OTA's. Resolution achievable using  $M = 16$  (3-bit quantization) is similar to that obtained with  $M = 22$  (single-bit quantization) (Fig.3), but power per opamp may be 35% higher in the latter. Note that this increase would be higher for the whole converter because multiple-of-two decimation is simpler to implement.

#### 4. Illustrative results

Fig.6 shows a microphotograph of a 4th-order 2-1-1 cascade multi-bit  $\Sigma\Delta$  fabricated in a  $0.7\mu\text{m}$  CMOS poly-diffusion caps technology [6]. This modulator was designed to fulfill the requirement of ADSL system: >12bit resolution at 2.2MS/s Nyquist rate. It uses the architecture of Fig.2 with 3-bit quantization in the last stage and single-bit quantization in the rest; oversampling ratio is 16 (35.2-MHz sampling rate) and reference voltages are  $\pm 2\text{V}$ . Integrator weights are in first column of Table 2. Main circuit limitations are shown in Table 3. As the worst-case equivalent load per opamp is considerably larger for the last-stage opamp, whose output drives the 3-bit (7 comparison stages) flash ADC, the opamp (a folded-cascode OTA) used for the first two stages was



**Fig. 6.** Die microphotograph (area =  $1.3\text{mm}^2$ ).



**Fig. 7.** Measured in-band  $SNDR$  against input level; large input region detail for 20samples.

scaled (2:1) for the last two. 3-bit DAC was implemented using a poly resistive ladder. Fig.7 shows the measured signal-to-(noise+distortion) ratio ( $SNDR$ ) obtained after decimation ( $\div 16$   $FIR$  filter implemented by software) as a function of the input level.  $SNDR$  peak is 74dB while dynamic range is 79.5dB, equivalent to 13-bit effective resolution. Power consumption for the modulator and clock phase generator is 55mW.

**Table 3.** Main circuit non-idealities

Opamp DC-gain	75dB (60dB required)
Unitary capacitor (pF)	0.5 ( $\sigma_{cr} = 0.15\%$ )
Equivalent load per opamp (pF)	6.1, 5.8, 7.5, 11.6
Opamp transconductance (mA/V)	4.8 (1st,2nd); 7.4 (3rd,4th)
Opamp output current (mA)	0.7 (1st,2nd); 1.35 (3rd,4th)
Opamp total output swing	5.3V (4V required)
3-bit DAC $INL$	1.5%FS

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