A Proposal for Hybrid Memristor-CMOS Spiking Neuromorphic Learning Systems

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***Abstract*—Recent research in nanotechnology has led to the practical realization of nanoscale devices that behave as memristors, a device that was postulated in the seventies by Chua based on circuit theoretical reasonings. On the other hand, neuromorphic engineering, a discipline that implements physical artifacts based on neuroscience knowledge, has related neural learning mechanisms to the operation of memristors. As a result, neuro-inspired learning architectures can be proposed that exploit nanoscale memristors for building very large scale systems with very dense synaptic-like memory elements. At present, the deep understanding of the internal mechanisms governing memristor operation is still an open issue, and the practical realization of very large scale and reliable "memristive fabric" for neural learning applications is not a reality yet. However, in the meantime, researchers are proposing and analyzing potential circuit architectures that would combine a standard CMOS substrate with a memristive nanoscale fabric on top to realize hybrid memristor-CMOS neural learning systems. The focus of this paper is on one such architecture for implementing the very well established Spike-Timing-Dependent-Plasticity (STDP) learning mechanism found in biology. In this paper we quickly review spiking neural systems, STDP learning, and memristors, and propose a hybrid memristor-CMOS system architecture with the potential of implementing a large scale STDP learning spiking neural system. Such architecture would eventually allow to implement real-time brain-like processing learning systems with about 10^8 neurons and 10^{12} synapses on one single Printed Circuit Board (PCB).**

I. Introduction

Neuromorphic engineering is an interdisciplinary discipline that takes inspiration from biology, physics, mathematics, computer science and engineering to design artificial neural systems, the physical architecture and design principles of which are based on those of biological nervous systems.

In neuromorphic engineering, technology and neuroscience cross-fertilize each other. This way, recently fabricated real memristor devices [1]–[4] (postulated since 1971 [5]–[7]) have been related to the mechanism known as Spike-Time-Dependent-Plasticity (STDP) [8]–[12], [14] which describes a neuronal synaptic learning mechanism that refines the traditional Hebbian synaptic plasticity model proposed in 1949 [16]. This combination of knowledge results in the proposal of potential artificial architectures for STDP learning systems [17]–[20], [54], [55], [77]. STDP was originally postulated as a family of computer learning algorithms [8], [9], and is being used by the machine intelligence and computational neuroscience community [12], [14]. At the same time its biological and physiological foundations have been reasonably well established during the past decade [21], [22].

In this paper we first describe some interesting concepts and properties behind spiking neural networks, also called Event-Driven neural systems, focusing on vision sensing and processing. Then we quickly review STDP (Section III) and memristor (Section IV) concepts. Afterwards, in Section V, we explain how the memristive mechanism, and one particular formulation of it, can explain the experimental characterization of the STDP phenomena in biological synapses. We will see how the shape of action potentials is a crucial component which influences and defines the mathematical learning of STDP, and how by changing action potential shapes the STDP learning rule can be modulated and changed. Section V also proposes circuit techniques for achieving STDP learning neural systems using memristors as synapses. In Section VI we describe how by exploiting present day AER (Address Event Representation) technology it is feasible to build hybrid CMOS/memristive scalable and reconfigurable neural systems with potential of assembling in the order of 10^8 neurons in one printed circuit board (PCB). Finally, Section VII discusses practical limitations.

II. Spiking Neural Networks for Event-Driven Sensing and Processing

For sake of clarity we will illustrate spike-based or event-driven (ED) sensing and processing within the domain of vision, but the principles described here extend to all other sensory domains and to new asynchronous ED computing paradigms. State of the art in artificial vision is based on video streams, by capturing sequences of images at a given "frame rate" and processing them frame after frame by computational algorithms. Frame-by-frame processing is CPU-hungry and always includes the latencies of sensing, transmitting and processing each frame. On the other hand, biological vision is frame-free: nor the eyes nor the brain have a clue of what a video frame is. In biology, retina cells (pixels) respond to external stimulation asynchronously sending action potential ("spikes" or "events") to the brain through the optical nerve fibers. Cells in the brain process these spikes through complex hierarchical structures to achieve, for example, shape size and position invariant object recognition. There are no frames, but a continuous flow of events from the retina through the cortical brain structures. Each neuron autonomously decides when to send out an event depending on the spatio-temporal collection of the received events. This asynchronous frame-free sensing and processing is what we call here "event-driven", ED, (as opposed to "frame-driven"). In humans, object recognition can be performed as quickly as in about 150ms [23], giving time to each neuron in the ventral stream hierarchy to fire just one spike [23], revealing a highly efficient timing-domain signal encoding in the brain. Based on these observations, neuromorphic researchers world-wide have developed in the

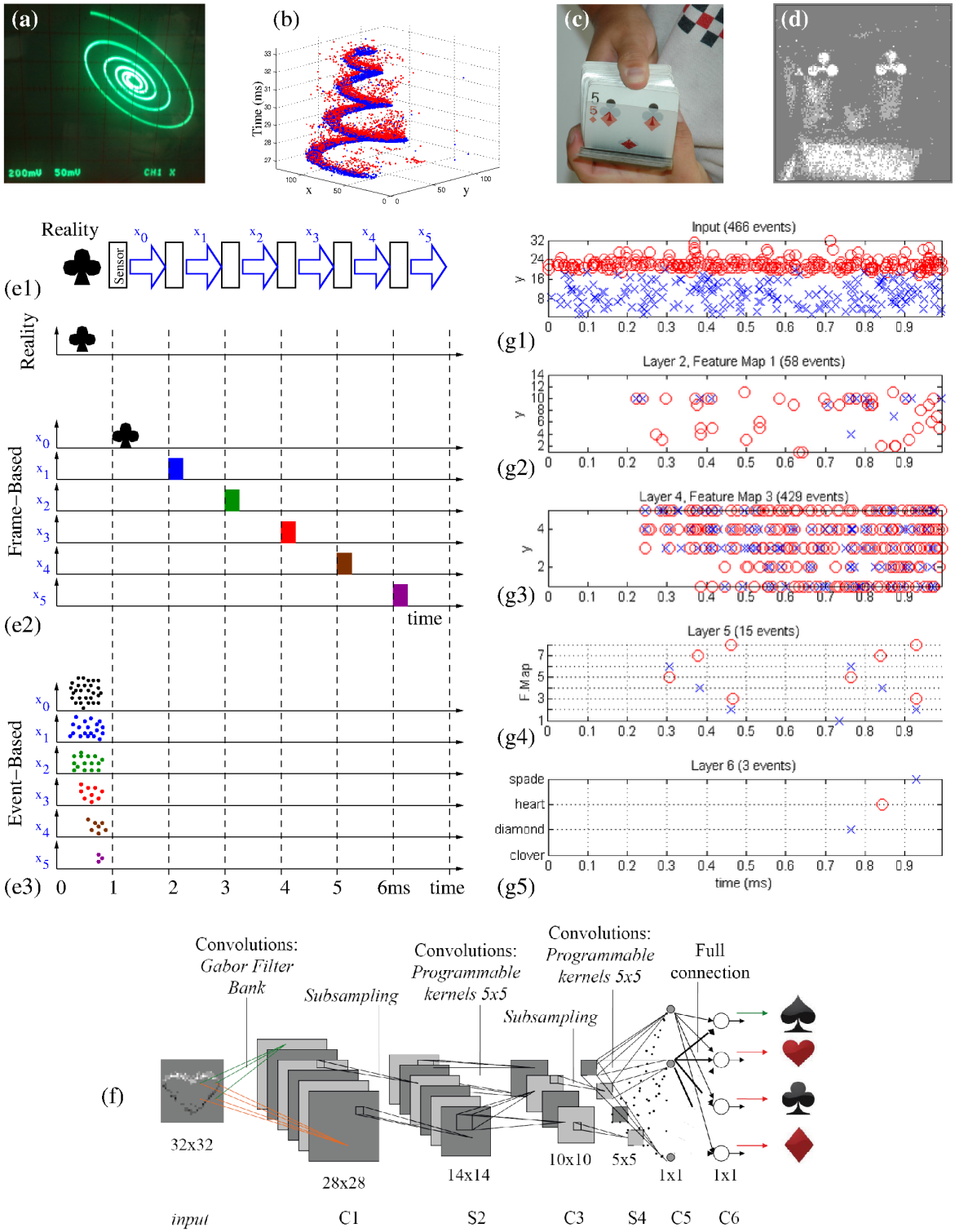

Fig. 1. Illustration of ED (event-driven) sensing and processing. (a) 500Hz spiral displayed on an analog oscilloscope, and (b) events (x,y,t) captured from an ED artificial retina (DVS) during 6ms. (c) Poker card deck browsed quickly, and (d) events captured during 3ms with a DVS and displayed in the (x,y) plane. (e) Comparison of frame-driven vs. event-driven vision sensing and processing: (e.1) a symbol is flashed during 1ms, captured by a sensor, and processed by 5 sequential stages; (e.2) in a frame-driven system with 1ms frame-time, the sensor needs 1ms to capture reality, and each processing stage requires a frame-time delay (assumed also 1ms) for processing; (e.3) in an ED sensing and processing system the sensor generates events as it observes reality, and these events are processed by the first stage "as they flow"; the output events of each stage are also processed by the next stage "as they flow", making it possible to achieve recognition while the sensor is still capturing the 1ms flash; (f) 5-layer ED Convolutional Neural Network (ConvNet)for recognizing poker card symbols when browsing a card deck; (g) Simulation results of the ConvNet in (f) using DVS recorded data representing 1ms events and describing each convolution unit using parameters from real convolution chips.

last 10 years a collection of ED sensor [24]–[32] and processor [33]–[38] chips. For example, Fig. 1 illustrates the basic principle of ED sensing and signal encoding, by showing the characteristics of one of the most popular ED vision sensors, the "Dynamic Vision Sensor" (DVS) [26]–[29] and used in a variety of applications [19], [39]–[54]. Whenever a pixel senses a change of light above a threshold it sends out of the chip an "event" in the form of a digital word (x, y, p) representing its address (x, y) and a polarity bit p (positive for a dark to bright change and negative for a bright to dark change), that typically needs fractions of a micro-second to be communicated. The DVS output consists of an asynchronous flow of events, known as AER "Address Event Representation". Fig. 1(b) shows the output event flow produced by a DVS chip when observing the 500Hz spiral shown in Fig. 1(a) for 6ms. Each event is represented as (x, y, p, t), where the polarity is denoted with color (blue for negative events and red for positive ones). The observed dynamic scene in Fig. 1(a) is thus represented by the frame-free event flow in Fig. 1(b). As can be seen, the ED DVS sensor provides very rich temporal information within these 6ms with sub-microsecond precision. Furthermore, such high temporal resolution was captured with the ambient light produced by the oscilloscope [26]. Physically, inter-chip AER communication typically uses a high speed digital multi-bit parallel bus, where one bit is used for 'p' (polarity) and the rest for (x, y), together with handshaking signals for asynchronous communication. Alternatively, serial AER schemes have also been proposed where a differential microstrip communicates (x, y, p) events bit-serially and asynchronously [56]–[58].

The availability of ED sensing and processing chips has allowed the implementation of the first ED sensory systems [34], [35], [41] that show the unique pseudo-simultaneity property, where the input and output event flows of a processing stage are (in practice) simultaneous or coincident in time. This is illustrated in Fig. 1(e-g) where a 5-layer structure of a feed-forward Convolutional Neural Network (ConvNet) [59] typically used for size and pose invariant object recognition, handwritten character recognition, scene recognition for robots, etc., is used. Fig. 1(e1) and Fig. 1(f) show schematically this 5-layer ConvNet. If this ConvNet is implemented using traditional Frame-driven sensing and image processing computing hardware [60], each stage has to wait until the output image from the previous stage is available. Fig. 1(e2) shows the latencies in a frame-driven system when a symbol is quickly flashed (in 1ms) to the camera sensor. A total of 6 frame delays (each 1ms) are needed for recognition. On the contrary, Fig. 1(e3) shows the situation for an ED implementation. An ED processor module processes events as they flow in, with a delay typically in the 100ns range per event [35]. The system does not need to wait for collecting image frames, but output events are emitted while the input events are processed as soon as enough input events are received, as is in cortical circuits. For orientation extraction, a 2D Gabor filter can produce an output event after just 4 to 6 correlated input events, signalling the presence of an oriented edge in that location at that time, producing an output that is almost simultaneous to the input event flow (with the delay of a few events). We call this the **pseudo-simultaneity** property between input and output event flows in an ED processing system. Thanks to the pseudo-simultaneity property the output events of all stages are available concurrently to the sensor output event flow (which is concurrent to reality), and correct object recognition is feasible while the sensor is still producing events. This pseudo-simultaneity property has already been verified experimentally with cascades of available ED convolution chips [35], with large arrays of ED convolution modules implemented within high-end FPGAs [40], and has been verified by simulations of full feed-forward ConvNets processing high speed DVS recordings, achieving symbol recognition with 1 to 2ms delays [41], as shown in Fig. 1(g). Fig. 1(g) shows the detailed ED processing during a 1ms flash of poker symbol "club" for the ConvNet in Fig. 1(f), displaying the individual positive (red circles) and negative (blue crosses) events at the retina output, at internal layers 2 4 and 5, and at the output category layer. As can be seen, correct recognition is available 0.84ms after stimulus onset.

Consequently, spiking (or ED) neural sensing and processing systems present interesting features inherited from their biological counterparts. However, for proper recognition, neural networks need to be trained and correctly learn the intended application. Spiking neural networks can be trained using the Spike-Timing-Dependent-Plasticity learning rule, which can be implemented using memristors. This is the subject of the rest of this paper.

III. Spike Timing Dependent Plasticity

Spike-timing-dependent plasticity (STDP) is a family of learning mechanisms originally postulated in the context of artificial machine learning algorithms (or computational neuroscience), exploiting spike-based computations (as in brains) with great emphasis on the relative timings of spikes. Gerstner started to report the first spike timing dependent learning algorithms [8] in 1993. STDP has been shown to be better than Hebbian correlation-based plasticity at explaining cortical phenomena [15], and has been proven successful in learning hidden spiking patterns [13] or performing competitive spike pattern learning [14].

Fig. 2 shows two neurons connected by a synapse. The pre-synaptic neuron is sending a pre-synaptic spike $V_{mem-pre}(t)$ through one of its axons to the synaptic junction. Neural spikes are membrane voltages from the outside of the cellular membrane V_{pre^+} with respect to the inside V_{pre^-}. Thus $V_{mem-pre} = V_{pre^+} - V_{pre^-}$ and $V_{mem-pos} = V_{pos^+} - V_{pos^-}$. The "large" membrane voltages during a spike (in the order of a hundred mV) cause a variety of selective molecular membrane channels to open and close allowing many ionic and molecular substances to flow, or preventing them from flowing through the membrane. Each synapse is characterized by a "synaptic strength" (or weight) w which determines the efficacy of a pre-synaptic spike in contributing to the cumulative action at the post-synaptic neuron. The synaptic weight w is considered to be non-volatile and analog in nature, but it changes in time as a function of the spiking activity of pre- and post-synaptic neurons. This phenomenon was originally

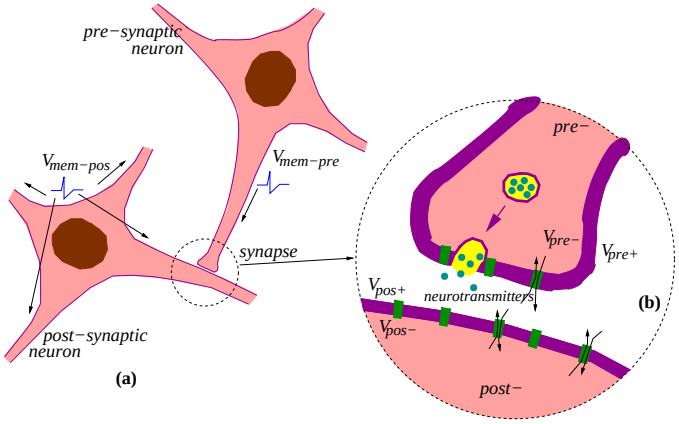

Fig. 2. Illustration of synaptic action. (a) A synapse is where a pre-synaptic neuron "connects" with a post-synaptic neuron. The pre-synaptic neuron sends an action potential $V_{mem-pre}$ traveling through one of its axons to the synapse. The cumulative effect of many pre-synaptic action potentials, generates a post-synaptic action potential at the membrane of the post-synaptic neuron, which propagates through all the neuron's terminations. (b) Detail of synaptic junction. The cell membrane has many membrane channels of varying nature which open and close with changes in the membrane voltage. During a pre-synaptic action potential vesicles containing neurotransmitters are released into the synaptic cleft.

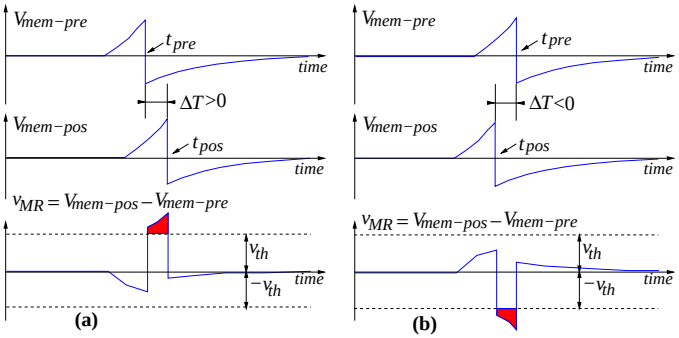

Fig. 3. Membrane voltage waveforms. Pre- and post-synaptic membrane voltages for the situations of positive ΔT (a) and negative ΔT (b). Voltage v_{MR} is the difference between the post-synaptic membrane voltage $V_{mem-pos}$ and the pre-synaptic membrane voltage $V_{mem-pre}$.

observed and reported in 1949 by Hebb [16]. Traditionally, this was described by computational neuroscientists and machine learning computer engineers as producing an increment in synaptic weight Δw proportional to the product of the mean firing rates of pre- and post-synaptic neurons. STDP is a refinement of this 1949 rule which takes into account the precise relative timing of individual pre- and post-synaptic spikes, and not their average rates over time. In STDP the change in synaptic weight Δw is expressed as a function of the time difference between the post-synaptic spike at t_{pos} and the pre-synaptic spike at t_{pre} (see Fig. 3). Specifically, as is shown in Fig. 4, $\Delta w = \xi(\Delta T)$, with $\Delta T = t_{pos} - t_{pre}$. The shape of the STDP function ξ can be interpolated from experimental data from Bi and Poo as shown in Fig. 4(a) [22].

Most of the present day literature on STDP presents a learning function ξ which depends on ΔT but not on the actual weight value w. This type of weight-independent STDP learning rule is usually known as "additive STDP". Additive

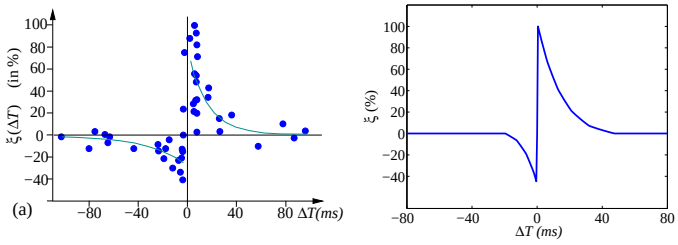

Fig. 4. (a) Experimentally measured STDP function $\xi(\Delta T)$ on biological synapses (data from Bi and Poo [22]). (b) Ideal STDP update function used in computational models of STDP synaptic learning.

STDP requires the weight values to be bounded to an interval because weights will stabilize at one of their boundary values [61]. On the other hand, in multiplicative STDP (mSTDP) [62] the learning function is also a function of the actual weight value $\xi_m(w, \Delta T)$. Furthermore, there usually appears a weight dependent factor which multiplies the original additive STDP learning function ξ_a, and which may generally be different for the positive ($\Delta T > 0$) and negative ($\Delta T < 0$) sides

$$\xi_m(w, \Delta T) = F(w, sign(\Delta T))\xi_a(\Delta T) \qquad (1)$$

In mSTDP weights can stabilize to intermediate values inside the boundary definitions. Thus, it is often not even necessary to enforce boundary conditions for the weight values [61]. Normally, factor $F(w, sign(\Delta T))$ is considered proportional to w. However, one may consider it to be proportional to w^a. As we will see later, some memristors yield a multiplicative type of STDP with power $a = 2$ (quadratic STDP), while other memristors result in plain additive STDP (with $a = 0$).

IV. Memristance

Memristance was postulated in 1971 by Chua [5] based on circuit theoretical reasonings. According to circuit theoretical fundamentals, there are four basic electrical quantities [7]: (1) voltage difference between two terminals "v", (2) current flowing through into a device terminal "i", (3) charge flowing through a device terminal or integral of current $q = \int i(\tau)d\tau$, and (4) flux or integral of voltage $\phi = \int v(\tau)d\tau$. A two-terminal device is said to be canonical [7] if either two of the four basic electrical quantities are related by a static relationship. A resistor has a static relationship between terminal voltage v and device current i. A capacitor shows a static relationship between charge q and voltage v. An inductor has a static relationship between its current i and flux ϕ. The memristor would show a static relationship between charge q and flux ϕ. Although none of the so-far reported memristors can be described by a static constitutive relationship in the (q, ϕ) plane (and thus, strictly speaking, the 1971 fourth canonical element is still missing), they all fall within Chua's 1976 generalization of *Memristive Systems* [6]. From here on we will use the term *memristor* for Chua's 1976 definition of *memristive system*.

Memristance has recently been demonstrated in nanoscale two-terminal devices, such as certain titanium-dioxide [1], [2], [63], [64] and amorphous Silicon [4] cross-point switches. However, memristive devices were reported earlier by other

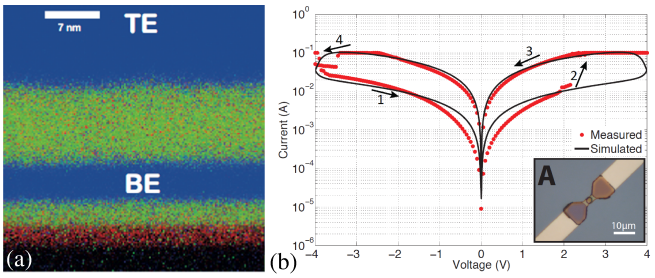

Fig. 5. Solid-state TiO_2-based memristors fabricated at Imperial College London. (a) CHEMI-STEM map of a lamella cross-section of a memristor: blue denotes Pt (top and bottom electrodes) while green and red correspond to Ti and O_2 species. (b) Simulated and measured pinched hysteresis I-V characteristics.

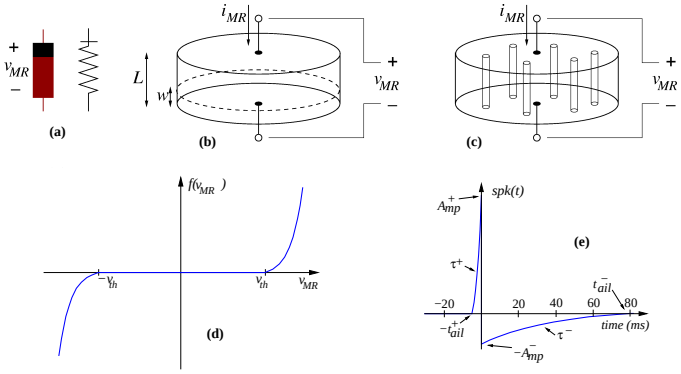

Fig. 6. (a) Memristor asymmetric symbols. (b) Illustration of moving wall model describing memristor operation as two variable resistors in series. (c) Illustration of filament formation/annihilation model describing memristor operation as two variable resistances in parallel. (d) Shape of memristor weight update function $f(v_{MR})$, (e) spike shape waveform.

groups [65]–[67]. Memristance arises naturally in nanoscale devices because small voltages can yield enormous electric fields that produce the motion of charged atomic or molecular species, changing structural properties of a device (such as its doping profile) while it operates. As an illustration, Fig. 5 shows results from planar TiO_2 memristors fabricated at Imperial College. Fig. 5(a) shows a cross-section of a memristor sandwiched between two platinum electrodes in blue (TE -top electrode- and BE -bottom electrode-), while green and red correspond to Ti and O_2 species. Fig. 5(b) shows the measured and simulated hysteresis I-V characteristics.

Memristors are asymmetric two-terminal passive devices. Consequently, their circuit symbol must indicate somehow their polarity. Fig. 6(a) shows two possible symbols. By definition, memristors can be either voltage/flux driven or current/charge driven. Here we will consider only Voltage/flux driven memristors, which can be described by [6]

$$i_{MR} = G(w, v_{MR}, t) v_{MR} \quad (2)$$

$$\dot{w} = f(w, v_{MR}, t) \quad (3)$$

Parameter w represents some *structural* property parameter of the memristor. For example, in the 2008 HP paper [1] the operation of the reported memristor was postulated as described by the *moving wall model* depicted in Fig. 6(b). In this simplified model a memristor of height L, sandwiched between two electrodes, has a low resistance region of height w and a high resistance region of height $L-w$. The memristor is considered to be divided into two regions. Both regions are separated by a boundary wall at position w, which moves up and down with the amount of charge that has flown through the memristor (in the case of being current/charge driven) or the accumulated flux (in case of being voltage/flux driven). The memristor would behave as two variable resistors in series. The total effective resistance of the memristor would be described by

$$R = R_{ON}\frac{w}{L} + R_{OFF}\left(1 - \frac{w}{L}\right) \quad (4)$$

This *moving wall model* can approximate phenomena like migration of oxygen ions [68] and vacancies [69], the lowering of Schottky barrier heights by trapped charge carriers at interfacial states [70], and the phase-change in some PCM (phase change materials) devices [71].

However, resistive switching effects in dielectric-based devices have normally been assumed to be caused by conducting filament formation across the electrodes, although the understanding and modeling of these phenomena remains controversial [72]. As a matter of fact, some researchers are observing the formation and annihilation of nanoscale width conducting filaments in memristors [73], [74]. However, let us here propose the following very simplified view to approximate this physical mechanism. Fig. 6(c) illustrates schematically a memristor with several conducting filaments between the two electrodes. The number of filaments or their cross-sectional area would increase or decrease with memristor operation. Let us call now w the total cross sectional area of the effective conducting filaments at a given instant in time, and S the total cross section area of the memristor. The filaments present high conductivity (low resistivity), while the bulk presents much lower conductivity (high resistivity). All formed parallel filaments behave as one effective resistance of low resistance, while the rest of the bulk behaves as another higher resistivity resistor. Therefore, now the memristor behaves as two variable resistors in parallel. Consequently, its total conductance (inverse of resistance) could be described as

$$G = G_{ON}\frac{w}{S} + G_{OFF}\left(1 - \frac{w}{S}\right) \quad (5)$$

where G_{ON} is the conductance per effective cross section area of the filaments, and G_{OFF} is the conductance per effective cross section area of the filament-less bulk material. Parameter w would change from 0 to w_{max}, the maximum possible effective cross section area of total conducting filaments ($w_{max} \leq S$). This changing cross section description not only approximates filament formation/annhilation phenomena, but also some other gradual cross section area variations observed in some phase-change or ferroelectric-domains-based materials [75]. As we will see later, a moving wall memristor yields quadratic STDP while a filament memristor yields additive STDP.

V. Memristors with CMOS Neurons for STDP

The STDP learning rule, as shown in Fig. 4, can be implemented by [18]–[20] (a) using a particular type of voltage/flux driven memristor [3] whose operation might be approximated by eqs. (2-3) with (see Fig. 6(d))

$$f(v_{MR}) = \begin{cases} I_o \ sign(v_{MR}) \left[e^{|v_{MR}|/v_o} - e^{v_{th}/v_o} \right] & if \quad |v_{MR}| \\ 0 & otherwise \end{cases} \tag{6}$$

and bounded synaptic strength $w \in [w_{min}, w_{max}]$, while (b) providing appropriately shaped pre- and post-synaptic spikes available at both synapse (memristor) terminals [19]. For example, consider a pair of identical pre- and post-synaptic spikes with a shape resembling that of biological spikes, with an on-set duration $|t^+_{ail}|$ and a tail of duration $|t^-_{ail}|$, as shown in Fig. 6(e),

$$spk(t) = \begin{cases} A^+_{mp} \frac{e^{t/\tau^+} - e^{-t^+_{ail}/\tau^+}}{1 - e^{-t^+_{ail}/\tau^+}} & if \quad -t^+_{ail} < t < 0 \\ -A^-_{mp} \frac{e^{-t/\tau^-} - e^{-t^-_{ail}/\tau^-}}{1 - e^{-t^-_{ail}/\tau^-}} & if \quad 0 < t < t^-_{ail} \\ 0 & \times \quad otherwise \end{cases} \tag{7}$$

Under these circumstances, memristor voltage is $v_{MR}(t, \Delta t) = \alpha_{pos} spk(t) - \alpha_{pre} spk(t + \Delta t)$ and from eqs. (3,6) synaptic strength update can be computed as

$$\Delta w(\Delta T) = \int f(v_{MR}(t, \Delta T)) dt = \xi(\Delta T) \tag{8}$$

which has been shown to result in the same shape illustrated in Fig. 4(b) [19]. Furthermore, by reshaping the spike waveform one can fine tune or completely alter the STDP learning function $\xi(\Delta t)$, as illustrated in Fig. 7 [76]. This way, by building neurons with a given degree of shape programmability, it is possible to change the STDP learning function at will, depending on the application, or make it evolve in time as learning progresses.

Fig. 8(a) shows a way of interconnecting memristors and CMOS neurons for STDP learning. Triangles represent the neuron soma, being the flat side its input (dendrites) and the sharp side the output (axon). Dark rectangles are memristors, representing each one synaptic junction. Each neuron controls the voltage at its input (V_{post} in Fig. 8(b)) and output (V_{pre} in Fig. 8(b)) nodes. When the neuron is not spiking it forces a constant voltage at both nodes, while collecting through its input node the sum of input synaptic spike currents coming from the memristors, which contribute to changing the neuron internal state. When the neuron spikes, it sets a one-spike waveform at both input and output nodes. This way, they send their output spikes forward as pre-synaptic spikes for the destination synaptic memristors, but also backward to preceding synaptic memristors as post-synaptic spikes. Zamarreño et al. showed extensive simulations on these concepts [19]. For example, Figs. 7(f1)-(f2) illustrate the case where forward and backward spikes have opposite polarities, resulting in a symmetric STDP update function $\xi(\Delta T)$. Figs. 7(g1)-(g2) illustrate an example where forward and backward spikes are different, with the backward spike such that its positive part exceeds the positive memristor threshold ($v_{th} = 1.0$).

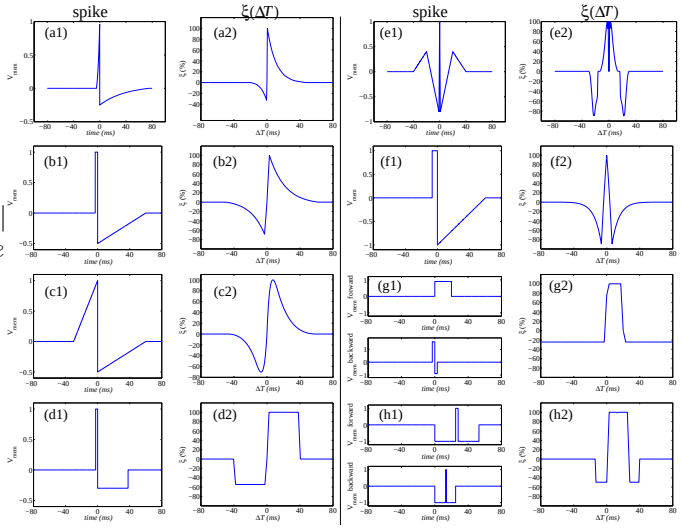

Fig. 7. Illustration of influence of action potential shapes on the resulting STDP memristor weight update function $\xi(\Delta T)$. Memristor upper and lower thresholds are normalized to amplitudes +/-1.0. From (a1)-(a2) to (e1)-(e2) the same spike waveform travels forward and backward. In (f1)-(f2) the forward and backward waveforms are the same but have opposite polarity. In (g1)-(g2) to (h1)-(h2) the forward and backward waveforms are different. In (g1)-(g2), the positive pulse of the backward waveform exceeds amplitude +1.0, thus producing negative STDP update whenever there is a post-synaptic spike alone (g2); otherwise if pre- and post-synaptic spikes happen within a given time window, there will be positive STDP update.

This produces LTD (long term depression) or negative STDP update whenever there is a post-synaptic spike sufficiently apart from a pre-synaptic one; and produces LTP (long term potentiation) if pre- and post-synaptic spikes happen within a given time window [54], [77]. Figs. 7(h1)-(h2) illustrate a similar STDP update behavior, except that update (whether positive or negative) is restricted to a constraint time window.

If the system is structured into neural layers (for example, Fig. 8(a) shows a 3-layer neuron system) with memristive synapses in between, then for each layer all pre-synaptic neurons should have the same forward spike shape and all post-synaptic neurons should have the same backward shape. This way, all memristive synapses between these two neural layers will have the same STDP function $\xi(\Delta T)$.

In all these circuits, synaptic strength is the conductance G of the memristor: the higher the conductance of a memristor G is (or the lower its resistance $R = 1/G$ is) the stronger the synaptic efficiency will be, as it will let more current through and thus affect more strongly the destination neuron state. Therefore, if the memristors used obey a "*moving wall*" model (see eq. (4)), then STDP update $\Delta w = \xi(\Delta T)$ changes wall position w, which from eq. (4) is directly proportional to resistance

$$\Delta R(\Delta T) = (R_{ON} - R_{OFF}) \frac{\Delta w(\Delta T)}{L} = \rho \xi(\Delta T) \tag{9}$$

where ρ is a constant. Consequently, synaptic strength $G = 1/R$ will change as

$$\Delta G(\Delta T) = -\frac{\Delta R(\Delta T)}{R^2} = -G^2 \Delta R(\Delta T) \propto -G^2 \rho \xi(\Delta T) \tag{10}$$

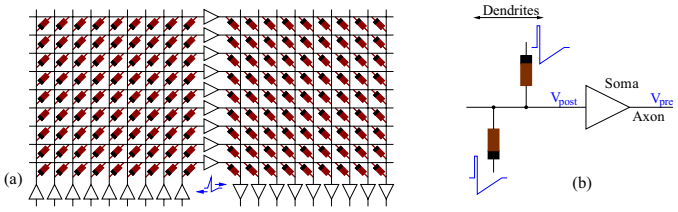

Fig. 8. (a) Example of Memristors and CMOS neuron circuits arrangement for achieving STDP learning: feed-forward neural system with 3 layers of neurons and two fully connecting synapse crossbars. (b) Details of parts around one post-synaptic neuron. While a neuron is silent, it sets a constant DC voltage at its input (V_{post}) and output (V_{pre}) nodes. When a neuron is sending a spike, it sets a voltage spike at both nodes. (c) Implementation of single spike STDP: Block diagram of CMOS neuron together with single memristor synapse connected between pre- and post-synaptic neurons, (d) example spike waveform with negative square neural activation shape, and (e) example spike waveform with positive more biological neural activation shape.

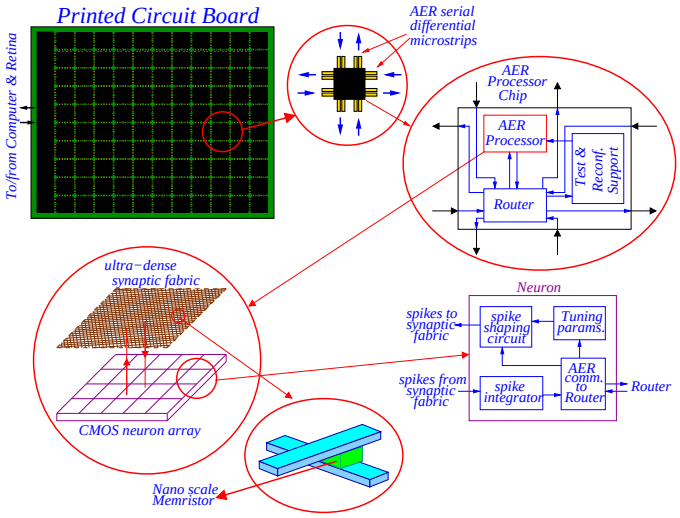

Fig. 9. Top down description of hybrid CMOS/nano multi-chip STDP Event-Driven system. A PCB holds a large number of chips arranged in a 2D grid communicating events serially through AER differential microstrip lines. Each chip contains an event-driven processor, a router, and test and configuration circuitry. The event-driven processor is made of an array of cells each containing one pre- and one post-synaptic neuron. On top of this array there would be two layers of perpendicular nanowires. At the crossing of two perpendicular nanowires there is memristive material implementing physically one synapse.

This means that synaptic strength update would follow a quadratic STDP learning rule.

If the memristor physics is better represented by the inter-electrode filament formation/annihilation model, then synaptic update would change parameter w of eq. (5), which is now directly proportional to memristor conductance (synaptic strength),

$$\Delta G(\Delta T) = \frac{G_{ON}}{S}\Delta w(\Delta T) = \gamma\xi(\Delta T) \qquad (11)$$

where γ is a constant. Therefore, synaptic update would be independent of actual weight (conductance) and the resulting STDP update rule is said to be of additive type. Note that eqs. (6)-(8) and the resulting functions $\xi(\Delta T)$ in Fig. 7 are common for both "wall" and "filament" models.

VI. Proposal for Scalable Spiking Neural Systems with STDP Learning Capability

Using present-day AER (Address Event Representation) CMOS technology it is quite feasible to build hybrid CMOS-memristor systems with many million neurons, once one could assemble reliably dense arrays of memristors on top of CMOS. This is illustrated in Fig. 9. On the top left we show a printed circuit board (PCB) hosting 110 identical AER chips, each communicating with its four neighbors through bidirectional bit-serial AER asynchronous links, for event-driven (spiking) communications. Each chip contains an AER processor, which in general is any array of neural processing units. This processor would receive events asynchronously, which shall be processed "as they flow", generating asynchronous output events. The chip also contains a block for programming and configuration of parameters, and a router block. The events interchanged between chips contain not only the standard Address Event (x, y, p) (where (x, y) is event coordinate and p its polarity), but also a header (a, b) indicating the chip address in the PCB. This chip address can indicate either the chip where the event was originated (source coding) or the destination chip (destination coding) [40]. The router block in each chip looks at the event header of each traveling event and decides whether to send it to its local event processor, or to one of its output ports. Similarly, for each event generated by the local event processor, the router adds a header and sends the event out through one of its output ports. The router takes all these decisions based on a local programmable routing table. The set of all routing tables in the array of chips in the PCB defines the architectural topology of the overall neural network.

In order to implement the STDP learning mechanism with memristors and spiking neurons as described throughout this paper, each AER processor in a chip may contain an array of CMOS cells, each containing an input and an output neuron. The input neuron sends out a spike of programmable shape whenever it is stimulated by an incoming event with its (x, y) coordinate. The output neuron receives and integrates incoming currents, and when it reaches its threshold sends out an Address Event with its (x, y) coordinate and polarity p, while at the same time sends a backward spike of programmable shape through its current summing input terminal. This current summing input terminal of the output neuron and the output terminal of the input neuron of each cell connect to a crossbar of nano-wires assembled on top of the CMOS chip using the connection arrangement known as CMOL [78]. At the crossing of each nano-wire pair there is memristive material implementing physically one memristor synapse. This arrangement would implement the scheme shown in Fig. 8.

VII. Practical Limitations, Realistic Sizes, Pitches, Density, Crosstalk and Power Considerations

Nanoscale memristor technology is still quite incipient and to the best of our knowledge no realistic large scale systems have been reported at the time of writing. However, we can

estimate an indicative scale and density of what may realistically be achieved in the near future, and the main limitations which may be encountered in a real physical implementation.

Regarding the wiring density of synaptic memristors, a pitch of $100nm$ is conservatively realistic for present day technologies [79], [80], while the near future might bring us closer to $10nm$ [81]. Assuming technologies of $100nm$ pitch 2D memristor arrays capable of interfacing reliably with lower CMOS become available some time soon, this would result in a synaptic density of 10^{10} synapses per cm^2. In the brain, the number of synapses per neuron is about 10^3 to 10^4. If we want to maintain the 10^4 ratio, we would need to fabricate CMOS neurons with a pitch of $10\mu m$, resulting in 10^6 neurons per cm^2. Such neuron sizes are quite realistic for present day nanometer scale CMOS (45nm or 32nm), given the complexity of the neurons needed. This would allow to have over 10^8 neurons and 10^{12} in the PCB of Fig. 9.

Another problem is that of resistance value ranges of the memristors' R_{min} (synapse ON) and R_{max} (synapse OFF). Reported memristors present resistance values from the $k\Omega$ range up to the $M\Omega$ range [2]–[4]. The memristor resistance value range affects the performance, reliability, crosstalk and power dissipation of a full large scale system. For example, it affects the driving capability of the neurons and their power consumption. If one neuron needs to drive 10^4 synapses of average value $1M\Omega$ to an average $1V$ level, it has to be able to provide an average current of $10mA$ during a spike (of say $20ms$), delivering $10mW$ per spike. If there are 10^6 neurons per cm^2 each firing at an average of $10Hz$ (which is similar to biological neurons), the synapses would dissipate a power of about $2kW$. The neurons would need at least the same power, presumably more. It is obvious that such a structure would melt quickly. The resistance range needs to be increased by a minimum factor of 100, so that minimum resistances are at least $100M\Omega$, or even larger. As pitches are lowered, resistances would need to increase quadratically with pitch decrease, to maintain the power limitation. Another option would be to scale down voltage, but there is not much range. Even our $1V$ maximum voltage assumption is quite optimistic for available present day memristors, which tend to operate between $2 - 10V$ [2]–[4]. Also, we have always assumed so far that voltage sources driving memristor terminals behave as ideal voltage sources, or at least, that the output resistance of such voltage sources is negligible compared to the total resistance they have to drive. Again, this will be achieved more easily if memristors present rather high resistance values. If driving voltage sources are no longer so ideal, then there will be crosstalk between lines. For example, if a spike is sent to a column then the voltage on all rows would change slightly. The consequence of this is that part of the charge provided by the incoming spike will be lost through non desired synapses and the impact of the spike on the target neurons will be weaker. During learning, the situation is less severe because for STDP update the memristor voltage has to exceed the learning threshold (v_{th} in eq. (2)). The effect of having non-ideal voltage sources is that the terminal voltage difference on the memristors needing synaptic update would be slightly less than in the ideal situation and learning would be weaker than expected ideally. However, having non-ideal voltage sources would not induce STDP update in undesired synapses. Another parasitic issue related to crosstalk is parasitic capacitive crosstalk between lines, which can be more pronounced as pitch and line distances decrease.

Also, one highly critical aspect which needs to be evaluated is the influence of component mismatches. Nanoscale devices suffer from high mismatch in general. Consequently, we should expect nanoscale memristors too to suffer from great parameter variations from one to another. It is true that they will operate as adaptive devices that will learn their functionality hopefully compensating for (some) mismatches. However, their learning and adaptation rules will also suffer from mismatch, making some synapses learn faster than others, or in slightly different fashions. In any case, the main sources of mismatch in memristor devices still need to be identified, and then their influence in the overall system learning behavior evaluated. However, to undertake such an initiative, we first need ready access to large arrays of reliable memristors fabricated in a stable and repeatable manner.

In general, an important issue is precise memristor modeling. Throughout this paper we have assumed an idealized voltage-driven memristor ideal model. This is useful to devise possible system architectures to achieve a desired functionality, such as STDP learning. However, to estimate realistic performance figures of resulting systems, it will be necessary to include non-ideal effects, both of the memristors and companion CMOS circuits. In this paper, no high order effects have been modeled, such as those related to noise, mismatch, and other memristor non-idealities not yet reported.

VIII. Conclusions

In this paper we have shown that STDP learning can be induced by the voltage/flux driven formulation of a memristor device. We have used this formulation to develop fully asynchronous circuit architectures capable of performing STDP, by having neurons send their spikes not only forward but also backwards. We have seen that depending on the memristive mechanism taking place, the resulting STDP behavior can be of additive or quadratic type. We have shown how the shape of spikes is critical to achieve and modulate a specific STDP learning function. At the end we have also discussed possible limitations of present day memristors.

The presented results are ideal extrapolations based on behavioral simulations. As memristor devices are further developed and non-ideal effects become known, the impact of non-idealities in the presented architectures and methods can be further assessed. Future work has to evolve towards more realistic memristor models and improved memristor devices, specially devices with much higher resistivities. One critical property that memristors need to provide for efficient STDP and non-volatility is the central dead-zone in Fig. 6(b). Another issue relates to the quadratic type of multiplicative STDP followed by the presented devices and architectures. This is a quite unusual form of STDP, which needs to be further investigated from a theoretical point of view. Similarly, since the presented approach allows the shape of the neural

spikes, and therefore the shape of the STDP learning curves to be changed in time, further theoretical studies are required to incorporate time varying STDP learning functions for speeding up, stabilizing, or in general improving learning performance.

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