The Stochastic I-Pot: A Circuit Block for Programming Bias Currents

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***Abstract*—In this brief, we present the "Stochastic I-Pot." It is a circuit element that allows for digitally programming a precise bias current ranging over many decades, from pico-amperes up to hundreds of micro-amperes. I-Pot blocks can be chained within a chip to allow for any arbitrary number of programmable bias currents. The approach only requires to provide the chip with three external pins, the use of an external current measuring instrument, and a computer. This way, once all internal I-Pots have been characterized, they can be programmed through a computer to provide any desired current bias value with very low error. The circuit block turns out to be very practical for experimenting with new circuits (specially when a large number of biases are required), testing wide ranges of biases, introducing means for current mismatch calibration, offsets compensations, etc. using a reduced number of chip pins. We show experimental results of generating bias currents with errors of 0.38% (8 bits) for currents varying from 176 μA to 19.6 pA. Temperature effects are characterized.**

***Index Terms*—Analog circuits, current-mode circuits, current biases, low-power circuits, mismatch, programmable current sources, reference currents.**

I. Introduction

ANALOG circuits require, in general, a set of bias currents which are usually provided by a current reference circuit allocated somewhere at the periphery of the chip together with some current scaling and distribution circuitry [1], [2]. Many times, circuit designers would like to be able to fine tune some of the designed bias currents in order to compensate for process variations and components mismatches. In other occasions, when experimenting with new circuits, it is desirable to have large degrees of freedom to play with all available bias currents and test the circuits for wide ranges of operating conditions. Under these situations, the safest solution is to provide one external pin for each bias current, making accessible a transistor gate. This allows to connect all available gates to external potentiometers (or a *pot-box*) so that one can experiment freely in the lab with all combinations of biases. In practice, this approach is limited to a reduced number of freely adjustable biases, since the number of pins of a chip cannot grow arbitrarily. To overcome this problem, Hasler *et al.* introduced the E-Pot circuit block [3], which exploited floating gate and tunneling/injection circuit techniques to program nonerasable analog voltages onto gates of biasing transistors. However, floating gate and tunneling/injection techniques are still presently little reliable and complicated to use successfully in standard CMOS processes.

In this brief, we introduce an alternative approach, based on the use of what we call the "*Stochastic I-Pot*" concept. The "*Stochastic I-Pot*" is a digitally programmable current source which, from a reference current, can provide any desired current with high precision and down to pico-amperes. Each I-Pot cell includes a digital register to select a current range, a current value for this range, and a sign. I-Pot cells can be chained so that any arbitrary number of current biases can be generated and independently programmed. The number of external pins that a chip needs for characterizing and programming the chain of I-Pots is three, independent of the number of I-Pots assembled. Consequently, designers can include any arbitrary number of programmable current biases, with the only restriction of area consumption. In our particular implementation, in a 0.35-μm CMOS process, the I-Pot cell area is $130\ \mu\text{m} \times 68\ \mu\text{m}$, one third the area of the pad it replaces.

This flexible approach allows designers to include programmable currents not only for biasing but also for independently trimming critical mismatch sensitive components, or to fine tune time constants. For example, it becomes possible to trim independently the transconductance of operational transconductance amplifier (OTA-C)-based filters [4] by precisely matching time constants of the form C/g_m. For example, Fig. 1(a) shows a simple bandpass filter of transfer function $V_o(s)/V_{\text{in}}(s) = (as)/(s^2 + bs + \omega_o^2)$, where $a = g_{m1}/C_2$, $b = g_{m3}/C_2$, and $\omega_o^2 = (g_{m1}g_{m2})/(C_1C_2)$. If many of those filters have to be built in a chip (or different chips) with matched time constants between them, the trimming current sources I_{trim} can be used to generate precise bias currents for the transconductors, and this way fine tuning all time constants. Offsets of differential pairs can also be trimmed by adding programmable offset currents for each differential pair, as shown in Fig. 1(b). And, in general, the approach allows for great versatility in adjusting and trimming current mode based circuits [5]. In present day industrial design, however, the tendency is to avoid trimming, since this introduces important delays which increases prototype costs. However, in some high performance designs where compromises between contradicting figure of merits are impossible to achieve, because of component mismatchings, trimming can be exploited to yield satisfactory results.

Delbruck *et al.* have recently presented a programmable bias current generator [6], where from a single reference they feed a 24-bit binary splitter. This way they can generate very fine current values for the higher range, but as one approaches the lower end (pico-amperes) the resolution and precision degrades drastically. The approach presented in this brief uses programmable

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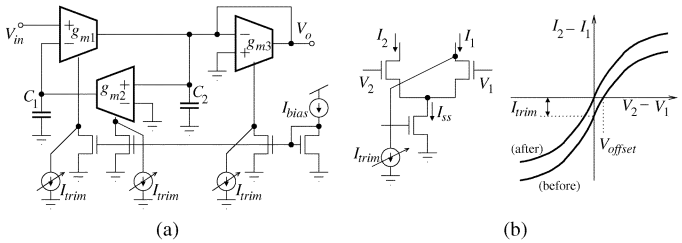

Fig. 1. Example illustration for (a) trimming time constants in an OTA-C filter using programmable bias currents, and (b) of differential pair offset trimming.

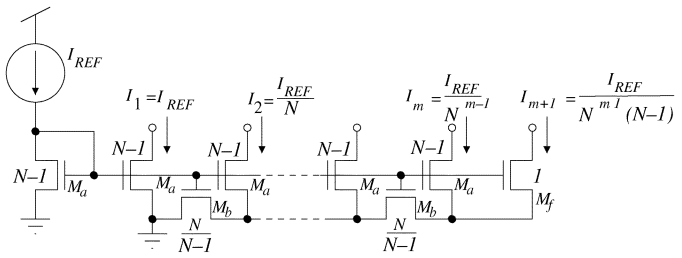

Fig. 2. Schematic of a generic MOS transistor based ladder structure that provides output currents ratioed by a factor N.

current ranges so that resolution is maintained throughout all decades, and we also include redundancy to improve precision.

In the next section we present the "*Stochastic I-Pot*" circuit, how to characterize it, and how to program it. Section III shows a particular implementation example, fabricated in the AMS 0.35-μm CMOS process, including experimental measurements that confirm a precision of 8 bits down to 19.6 pA. Section IV shows temperature effects.

II. "*Stochastic I-Pot*" Circuit Description

The "*Stochastic I-Pot*" circuit presented in this brief exploits the use of current mode ladder structures applied to MOS transistors [7], [8]. A generic MOS ladder structure, configured as current source, is shown in Fig. 2. All transistors are proportional to a unit size ratio W/L by either a factor 1, $N-1$, or $N/(N-1)$. This way, branch currents I_i have an attenuation ratio of N from each branch to the next one. In the "*Stochastic I-Pot*" circuit, we use two of these ladder structures.

The first ladder structure, with attenuation ratio around $N = 10$, selects an operating current range. This range ladder has 6 output branches, so that the output current can be selected between the input reference current $I_{\rm REF}$ and around $I_{\rm REF}/10^6$. In our particular implementation, we set $I_{\rm REF} = 100$ μA, so that the minimum range current is about 100 pA.

For the second ladder structure, we use an attenuation ratio of $N = 2$. This allows for selecting any binary combination of current branches, in the same way a current DAC would do. However, we do not want to have a high precision (like 8-bit) current DAC within each I-Pot, because they would require extremely large transistor sizes and would most probably not provide such precision for very small currents down to pico-amperes.

In our approach we use ladder structures with attenuation ratio $N = 2$, with a large number of branches, but with small transistor sizes so that we intentionally provide large mismatches between the current branches. By having a large number of branches, each with large mismatch, we achieve a good coverage of possible output current combinations. Consider a ladder (see Fig. 2) with input current $I_{\rm REF} = 300$ pA,

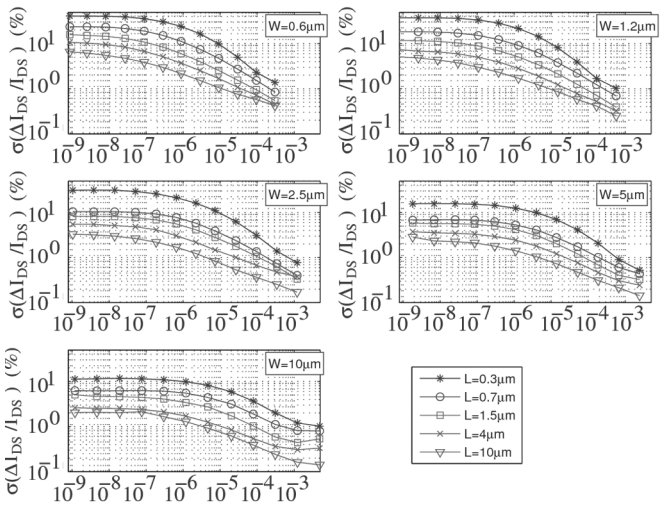

Fig. 3. Current mismatch standard deviation measurements, for nMOS transistors in a 0.35-μm CMOS process. Vertical axes represent standard deviation in %, and horizontal axes operating current. Measurements are taken for 30 different transistor sizes, by sweeping width {10, 5, 2.5, 1.2, 0.6} μm and length {10, 4, 1.5, 0.7, 0.3} μm

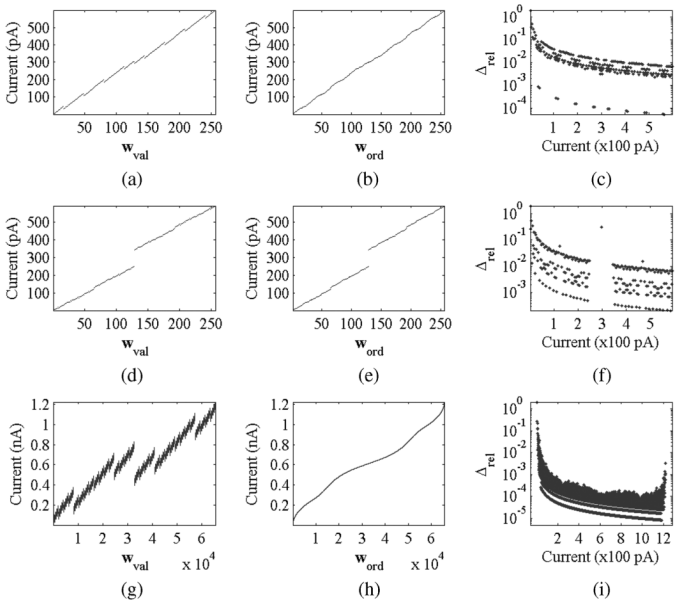

Fig. 4. (a)–(c) Illustration of mismatch effects in a MOS ladder with ratio $N = 2$. (d)–(f) Same, but for an "unlucky" ladder example. (g)–(i) Illustration of a ladder structure with duplicated output branches. (a), (d), (g) I-Pot output currents versus digital control word $\mathbf{w}_{\rm val}$, (b), (e), (h) same output currents after ordering versus $\mathrm{w}_{\rm ord}$, (c), (f), (i) relative difference between consecutive values.

attenuation ratio $N = 2$, eight branches, and a unit transistor of size $W/L = (1\ \mu\text{m})/(0.7\ \mu\text{m})$. For a transistor of this size, fabricated in the AMS 0.35-μm CMOS process, and driving a current of $\sim$700 pA, results in a current mismatch standard deviation of around $\sigma \approx 35\%$, as can be seen by interpolating the measurements shown in Fig. 3 [8], [9]. Fig. 4(a) shows the measured output current for such a ladder obtained as function of the 8-bit digital word $\mathbf{w}_{\rm val}$ that controls the combination of branches. As can be seen, this characteristic differs dramatically from a conventional stair-case that a high-precision 8-bit DAC would provide. However, suppose we introduce a look-up table between the digital word we provide and the one physically applied to the ladder structure, so that the output currents become

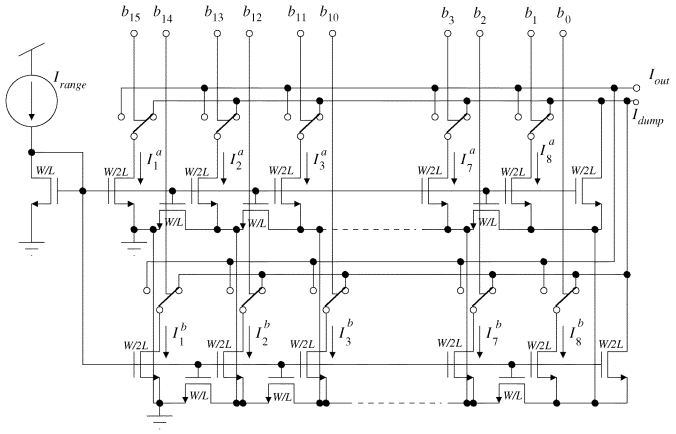

Fig. 5. Circuit schematic of ladder structure with attenuation ratio $N = 2$ and duplicated output branches.

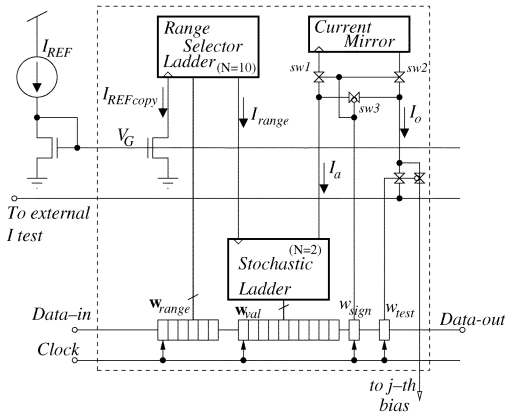

Fig. 6. Circuit diagram of complete I-Pot cell.

ordered. The result is shown in Fig. 4(b) for the same ladder and bias reference current. Now we see a monotonic increasing dependence between the digital control word $\mathbf{w}_{\rm ord}$ and the output current. It does not matter that this relationship is not perfectly linear. Our objective is simply to provide a bias current as close as possible to a desired value. Such objective is limited by the intervals between consecutive current values in Fig. 4(b). To characterize these intervals, we show in Fig. 4(c) the relative difference between the consecutive values in Fig. 4(b)

$$\Delta_{\rm rel} = 2\left|\frac{I_n - I_{n+1}}{I_n + I_{n+1}}\right|. \tag{1}$$

As can be seen, we have errors below 10% for the whole range except the first 1/20 of the range, and below 1% for last 1/4 of the range. But this was a "lucky" particular case. It is perfectly possible to find situations where the mismatch plays against us and we obtain an unfortunate extremely large maximum gap. This is, for example, the case illustrated in Fig. 4(d)–(f), for another I-Pot, exactly equal to the one used for Fig. 4(a)–(c). Such situations occur for example, when the maximum branch current I_1 in Fig. 2 results much larger than the sum of all the others. This produces an extremely large gap in the center of the characteristic. In Fig. 4(e) the largest gap was of 92.3 pA for a total range of 591.3 pA. Consequently, as can be seen in Fig. 4(f), current values in the range between 250 to 350 pA cannot be generated with a precision better than 30%.

One can think of several solutions to circumvent this problem. After playing with a few of them and testing them with statistical simulations, we found out that the most reliable solution is to duplicate the output branches of the ladder with attenuation ratio $N = 2$. This not only guarantees there will be no large gaps between consecutive current values, but at the same time reduces dramatically the value of the largest gap found, for the same transistor sizes and input reference current.

Fig. 4(g)–(i) shows the same situation for the circuit in Fig. 4(a)–(c), but where now the output branches are duplicated. Now there are 16 bits to select output branches combinations but the maximum current gap in Fig. 4(h) is now reduced to 0.20 pA, excluding the first and last 100-pA intervals of the range. The relative error is shown in Fig. 4(i). As can be seen it is less than 0.001 for currents between 137 and 1214 pA. Fig. 5 shows the complete circuit schematics of a ladder with attenuation ratio $N = 2$ and duplicated output branches. In case the lower current ranges need to operate below 10 pA or less, special sub-pA current mode techniques [10], [11] need to be employed for the second (stochastic) ladder structure, like introducing level shifting between drain and gate of the input transistor and connecting the ground voltage above substrate.

Fig. 6 shows the complete circuit diagram of a stochastic I-Pot cell. Each stochastic I-Pot receives a copy $I_{\rm REFcopy}$ of a common reference current $I_{\rm REF}$, which is the input to a pMOS $N = 10$ range ladder structure with 6 output branches. The common reference current can be generated by any bandgap type circuit [12] with temperature compensation, or provided off-chip through an extra pin. The digital word $\mathbf{w}_{\rm range}$ selects just one of the range ladder outputs (not a combination of them). This current $I_{\rm range}$ sets the coarse mode range of the I-Pot output current. Current $I_{\rm range}$ is now fed to the input of an nMOS $N = 2$ ladder structure with duplicated output branches. Let us call this ladder a "stochastic ladder", because from I-Pot to I-Pot there will be a high degree of randomness between the ladders. In our particular case we implement 16 (2×8) duplicated branches. The particular combination of output current branches is controlled by the digital word in register $\mathbf{w}_{\rm val}$. The output of this ladder I_a can be optionally sign inverted by transmission gates $sw1 - sw3$, controlled by the state of an extra register $w_{\rm sign}$, which inserts or not a pMOS current mirror in the output current path. Finally, the signed output current I_o is directed to either its destination bias point, or to a chip output pin $I_{\rm test}$ for characterization purposes, depending on the state of register $w_{\rm rest}$. All registers, $\mathbf{w}_{\rm range}$, $\mathbf{w}_{\rm val}$, $w_{\rm sign}$, and $w_{\rm test}$ are shift registers, connected in series, and clocked by the same clock signal. I-Pot cells can be chained directly in series by chaining their shift registers sharing all the same clock signal. All I-Pot cells share also the same gate line V_G and test line $I_{\rm test}$.

The main drawback of the present I-Pot approach is that each I-Pot of each fabricated chip needs to be characterized individually. The good news are that this is quite easy to do by using a host computer that loads the chained shift registers, while at the same time we require the use of just one single external current metering instrument.

The procedure for characterizing the I-Pots of a chip is as follows.

1) Each I-Pot has to be characterized individually. Consequently, the $w_{\rm test}$ bit of only one single I-Pot has to be set to "active." All others must be disabled. This way, only one single I-Pot output is connected to external line $I_{\rm test}$.
2) Sweep the two signs for the active I-Pot.

3) For the selected I-Pot and sign, sweep all current ranges through digital word $\mathbf{w}_{\rm range}$.
4) For the selected $\mathbf{w}_{\rm range}$, sweep all 16 output current branches, measure the selected branch current with the external current meter through pin $I_{\rm test}$, and store it in a file in the computer.

After completing the measurements for one I-Pot, we will have stored in the computer a total of $2\ \text{signs} \times 6\ \text{ranges} \times 16\ \text{branches} = 192$ current values per I-pot. Measuring one I-pot takes about two minutes. For each sign and range, we can now produce all 2^{16} possible combinations, order them, and store the mapping table from un-ordered to ordered sequence in a look-up table on the host computer. We will need one look-up table per range, sign, and I-pot. Using these look-up tables and a little program, a user can find the optimum value of $\mathbf{w}_{\rm val}$ and $\mathbf{w}_{\rm range}$ for a desired target bias current.

III. Experimental Results

A set of identical I-Pots was fabricated in the AMS 0.35-μm CMOS process. The stochastic ladder uses 16 duplicated output branches, and the unit transistor of the ladder structure has a size of $W = 1\ \mu$m, $L = 0.7\ \mu$m. This ladder was intentionally made with a small unit transistor to increase mismatch, and therefore improve its stochasticity. The range ladder used 6 output branches, and the input current to the range ladder was set to 100μA. The range ladder was designed according to Fig. 2 with an attenuation ratio of $N = 11$, approximately. Transistor sizes for the range ladder were $W = 10\ \mu$m, $L = 1\ \mu$m for transistors M_a, $W = 1\ \mu$m, $L = 1\ \mu$m for transistors M_b, and $W = 1\ \mu$m, $L = 1\ \mu$m for transistor M_f. Note that, according to Fig. 2, we did not use the exact correct sizing for transistors M_b, which should have been instead $W = 1.1\ \mu$m, $L = 1\ \mu$m. The consequence of this is simply that the attenuation factor between consecutive range currents will not be equal to 11, but will vary slightly. For us, this is not of critical importance, as long as a certain overlap between consecutive ranges is produced, as will be explained later. The I-Pot schematic, as shown in Fig. 6, includes a 24-bit shift register (6 bits for the range ladder, 16 bits for the stochastic ladder, one sign bit, and one test bit). It turns out that the most area consuming part of the I-Pot are these shift registers. Because of this we used a dynamic shift register. After loading the complete shift register, the data is copied into static latches. The resulting layout size of the fabricated I-Pot is 130 μm $\times$ 68 μm. When we designed this same I-Pot using a conventional static edge-triggered master-slave shift register, the size of its layout was 275 μm $\times$ 64 μm.

After measuring one of the fabricated I-Pots we obtain the currents shown in Fig. 7. Each of the six subgraphs corresponds to one of the available ranges provided by the range ladder. In each subgraph we have added the ordered version of the measured current values. This ordered version is drawn with the continuous line. The minimum and maximum current values provided by each range are as follows. First range [0.4 μA, 176μA], second range [30 nA, 12.7 μA], third range [1.9 nA, 673 nA], fourth range [126 pA, 44.0 nA], fifth range [9.9 pA, 3.28 nA], and sixth range [1.2 pA, 331 pA]. With the ordered measured values we can now compute the difference between them, according to (1). Fig. 8 shows these values, expressed in bits[1] as

[1] $1/2^{n_{\rm bits}} = \Delta_{\rm rel} \Leftrightarrow n_{\rm bits} = -\log_2(\Delta_{\rm rel}) = -(\ln \Delta_{\rm rel})/(\ln 2)$.

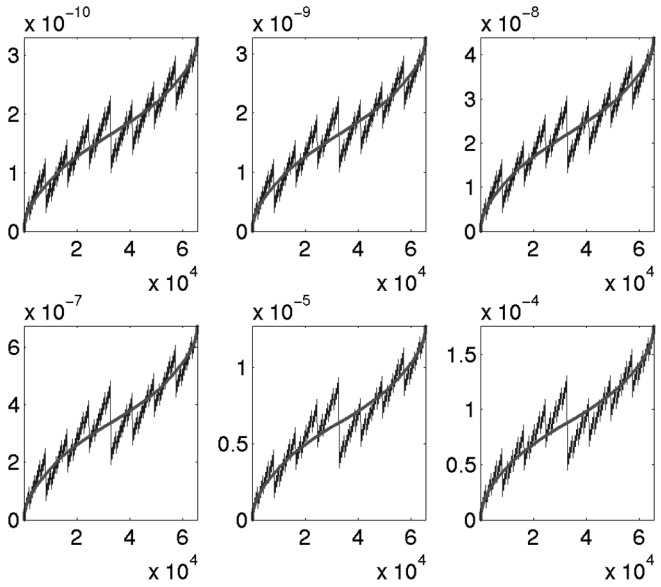

Fig. 7. Measured currents of one of the fabricated I-Pots for all six current ranges. Continuos lines show the same values after ordering. Vertical axes are measured currents, horizontal axes are index numbers for the $2^{16} = 65536$ measurements of each range.

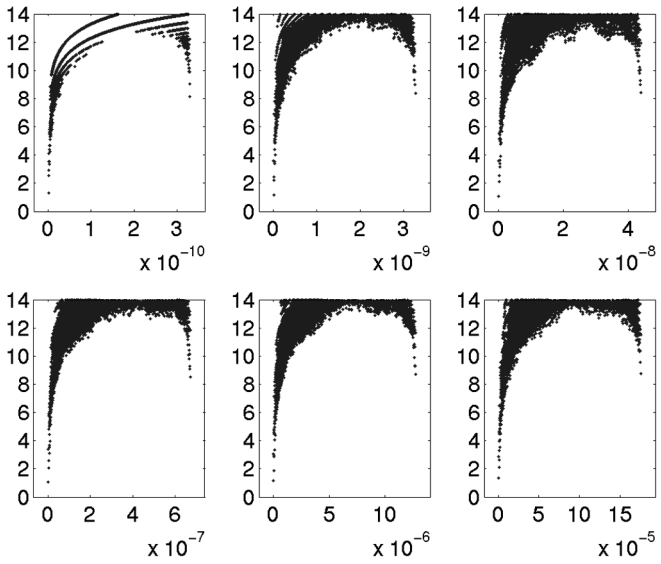

Fig. 8. Computed relative increments between ordered consecutive values (see eq. (1)), expressed in bits. Vertical axes are resulting bits, while horizontal axes are absolute measured currents.

function of currents. Striation effects can be observed, specially as current decreases, due to quantization effects in the data acquisition instrument.We can see that the maximum resolution is obtained for the central parts of the ranges, reaching values as high as 13 bits. On the other hand, for the external parts of the ranges the resolution decreases dramatically down to values as low as 1 bit. This is because in the central part of the ranges there is a higher density of redundant values than on the extremes of the ranges. However, if the ranges overlap, we can increase the density of redundant values and improve the resolution. The procedure is as follows. Let us take all the values of all six ranges and order them as one unique set of current values. Each current value is uniquely defined by its range and its 16-bit word

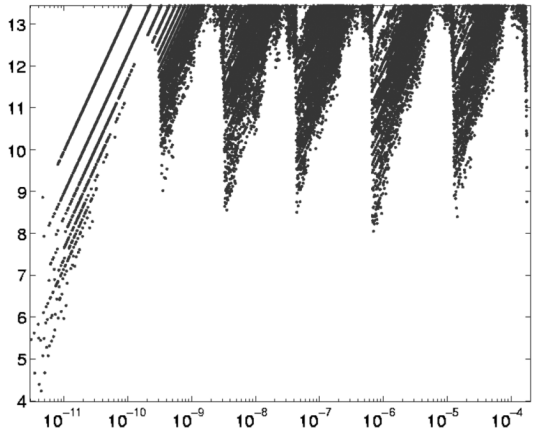

Fig. 9. Computed relative increments, expressed in bits, when considering all measured values of all six ranges as a unique set. Vertical axis represents resulting bits, while horizontal axis represents absolute measured current.

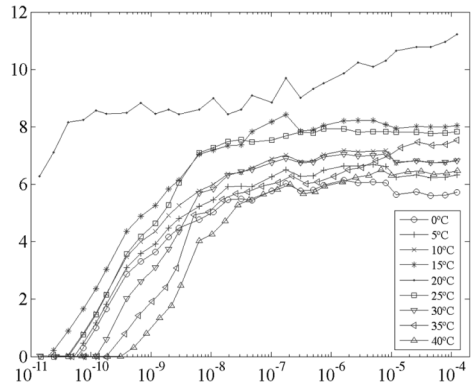

Fig. 10. Effect of temperature on precision.

within that range. Let us now compute the difference of consecutive values, as defined by (1), and express them in bits. The result is shown in Fig. 9. We can still see very well the regions of the six ranges with their respective maximum resolution central parts of up to 13 bits. However, the resolution of the extremes of each range has improved to values of above 8 bits. Neglecting the lower currents of the whole merged six ranges, the worst resolution is obtained for currents around 0.7 μA, yielding a resolution of 8.05 bits. The first current value showing a resolution above 8 bits is 19.6 pA, and the largest one 176 μA. Note that in the lower range for as low as 3 pA, the precision is still above 4 bits. Note also that what determines the worst case precision (neglecting the lower currents) is how evenly spaced are the range selector currents, or by how much the ranges overlap. For example, in Fig. 9, we can see that if we double the number of ranges from 6 to 12 (by using a range ladder with $N = 3.3$), the worst case precision will be around 11 bits.

Settling times have been characterized by simulations, with the I-Pot output node connected to a voltage source. One of the two LSB branches was switched from ON to OFF. For the top range the delay was less than 10 ns, and decreased exponentially to 10 ms for the smallest current range.

IV. Temperature Effects

Ideally speaking, since the I-Pot operation is based on current splitting techniques, the effect of temperature should be minor as long as the current division ratios between ladder branches remain unaltered. Unfortunately, this is not completely true, and those ratios do depend slightly on temperature. We have observed that those ratios can vary between 0.1% and around 1% for temperature variations between 0°–40 °C for currents above tens of *nano-amperes*. For lower currents the effect of temperature is more drastic, since leakage currents increase rapidly with temperature. Fig. 10 shows the error (expressed in bits) between the I-Pot current expected when characterized at 20 °C, and the one obtained when doing new measurements, sweeping temperature between 0 °C and 40 °C. Each data point is obtained by taking the maximum error within 1/30th of the 7-decade current range.

V. Conclusion

A compact, versatile, and powerful circuit for generating digitally controlled precise bias currents is presented. 8-bit precision has been verified from currents as low as 19.6 pA up to values of 176 μA (almost 7 decades). Temperature degrades precision gracefully, and is more severe for smaller currents. This circuit is specially handy for experimenting with current-mode circuits operating in weak inversion, where mismatch is high and operating range extends over several decades. It is also very useful for experimenting with new circuits, where it might be desirable to include a large number of (fine-)tunable current biases for trimming gains and offsets. The only drawback is that each I-pot needs to be characterized individually using an external off-chip current metering instrument.

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