A Bioinspired 128x128 Pixel Dynamic-Vision-Sensor

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***Abstract*—This paper presents a 128x128 dynamic vision sensor. Each pixel detects temporal changes in the local illumination. A minimum illumination temporal contrast of 10% can be detected. A compact preamplification stage has been introduced that allows to improve the minimum detectable contrast over previous designs, while at the same time reducing the pixel area by 1/3. The pixel responds to illumination changes in less than 3.6μs. The ability of the sensor to capture very fast moving objects has been verified experimentally. A frame-based sensor capable to achieve this, would require at least 100K frames per second.**

I. INTRODUCTION

Conventional image sensors are frame-based. In frame-based imagers the detected photocurrent is integrated in a capacitor during a fixed time period (the frame time). The reached voltage level of each pixel is communicated in a sequential way out of the chip. Biological vision sensors operate in a quite different way. When the activity level of a retina pixel reaches some threshold, the pixel sends a spike to its connected neurons. That way, information is sent out and processed continuously in time (in a frame-less way) and communication bandwidth is used only by active pixels. Highly active pixels send spikes faster and more frequently than less active ones. Event driven or Address-Event-Representation (AER) [1]-[3] bioinspired vision sensors have become very attractive in recent years because of their fast sensing capability, reduced information throughput and efficient in-sensor processing.

In this paper we present a very low latency AER-based temporal contrast vision sensor. Several prior frame-based temporal difference detector imagers have been published [4]-[8], however they suffer from limited speed response because they operate based on photocurrent integration during consecutive frames and computing the difference between them. Several event-based (frame-free) temporal contrast vision sensors have been reported in recent years [9]-[12]. They are also referred to as Dynamic Vision Sensors (DVS). The sensor published by Kramer [10] had low contrast sensitivity, while the one by Zaghloul [11] suffered from poor FPN (fixed pattern noise). Lichtsteiner et al. [9] presented the first practical DVS by introducing a self-clocked switched capacitor differencing and amplification stage resulting in low FPN (2.5%), practical contrast sensitivity (15%), reasonable pixel array size (128x128), very good latency (15μs), excellent intrascene dynamic range (120dB), and sufficient maximum event rate throughput (1Meps). The sensor was appropriate for high speed vision, since it could follow rotating objects up to a speed of 200 rps. Recently, a single pixel for a DVS sensor that achieves a 0.3% contrast sensitivity has been published [13]. The higher contrast sensitivity is achieved by a two-stage differencing amplifier [14], thus increasing the pixel gain a factor 50. However, this new design has very reduced pixel bandwidth.

This paper presents a new AER transient vision sensor (DVS) which is based on the one reported by Lichtsteiner and Delbrück [9]. By introducing a small area non-switched preampliflying stage we obtain a slightly better contrast sensitivity (10%) while reducing the pixel area by a 1/3 factor [15]. By using an alternative photo sensing stage, latency can be reduced down to 3.6μs. The price paid is an increase in the current consumption due to the preamplification stage and a smaller intrascene dynamic range. FPN also increases slightly but it remains significantly lower than the achieved contrast sensitivity. A mechanism has been designed to dynamically adapt the DC levels of the pixel preamplifying stage according to ambient illumination. Thanks to this adaptation mechanism the retina achieves a dynamic range higher than 100dB. However, intrascene dynamic range is reduced to 54dB.

II. SYSTEM DESIGN

The pixel presented in this paper is based on a previously reported design [9]. However, in the present design a preamplification stage has been introduced that allows to achieve a slightly improved pixel sensitivity while reducing pixel area.

Fig. 1(a) shows a conceptual block diagram of the pixel. The first stage, the photoreceptor stage, which is based on a gate-biased source-driven stage [17], converts photocurrent I_{ph} to voltage V_{ph}

$$V_{ph} = \frac{V_G}{n} + U_T \ln \frac{I_{ph}}{I_{sp}}, \qquad (1)$$

where n and I_{sp} are the substhreshold slope factor and the substhreshold current factor of transistor M_p [16]. In this type of source-driven stages, gate voltage V_G sets the DC level of the source voltage V_{ph} of transistor M_p for a given photocurrent I_{ph}.

The second stage, which is the new preamplification stage, is a voltage gain stage producing an output voltage

$$V_{pa} = V_{off} + GU_T \ln \frac{I_{ph}}{I_{sp}} \qquad (2)$$

being G the voltage gain of this preamplification stage and V_{off} a DC voltage. Voltage V_{pa} feeds a capacitive differentiator stage (as proposed in [9]) such that

$$dV_{diff} = -\frac{C_1}{C_2}dV_{pa} = -G\frac{C_1}{C_2}U_T d\ln\frac{I_{ph}}{I_{sp}} = -G\frac{C_1}{C_2}U_T\frac{dI_{ph}}{I_{ph}}. \qquad (3)$$

The capacitive ratio C_1/C_2 is designed to produce additional voltage amplification. Thus, total voltage amplification from V_{ph} to V_{diff} is $A = GC_1/C_2$. Voltage V_{diff} is compared to thresholds V_θ^+ and V_θ^-. When voltage V_{diff} exceeds the upper threshold V_θ^- (when light changes from I_{bright} to I_{dark}), a negative event is generated through channel OFF and node V_{diff} is reset to an intermediate reference voltage V_{REF}. When voltage V_{diff} decreases below the lower threshold V_θ^+ (when light changes from I_{dark} to I_{bright}), a positive event is generated through channel ON and node V_{diff} is reset to reference voltage V_{REF}.

Let us call $V_{diffON} = (V_\theta^+ - V_{REF}) + (V_{os} + V_{osn}) < 0$ the voltage excursion at node V_{diff} that generates a single positive event through the ON channel, where V_{osn} is the DC offset voltage of comparator A_{on} in Fig. 1(a), and V_{os} represents the DC offset voltage of amplifier A_d plus the systematic offset voltage introduced at its input node by switching. Similarly, $V_{diffOFF} = (V_\theta^- - V_{REF}) + (V_{os} - V_{osf}) > 0$ is the voltage excursion at node V_{diff} that generates a single negative event through the OFF channel, with V_{osf} being the DC offset voltage of comparator A_{off}. Referring to the input, let us call "ON contrast threshold" (or "ON contrast sensitivity") $\theta_{ev}^+ > 0$ the minimum contrast stimulus that generates a single positive event through output channel ON, and "OFF contrast threshold" (or "OFF contrast sensitivity") $\theta_{ev}^- > 0$ the minimum contrast stimulus that generates a single negative event through output channel OFF. By integrating equation (3),

$$\theta_{ev}^+ = \left|\ln\frac{I_{bright}}{I_{dark}}\right| = \left|\frac{V_{diffON}}{nU_TA}\right| = \left|\frac{(V_\theta^+ - V_{REF}) + (V_{os} + V_{osn})}{nU_TA}\right|$$
$$\theta_{ev}^- = \left|\ln\frac{I_{dark}}{I_{brigth}}\right| = \left|\frac{V_{diffOFF}}{nU_TA}\right| = \left|\frac{(V_\theta^- - V_{REF}) + (V_{os} - V_{osf})}{nU_TA}\right| \qquad (4)$$

That way, the minimum contrast stimulus to be detected can be adjusted through pixel threshold voltages V_θ^+ and V_θ^-.

The schematics of the small-area preamplifier stage are shown in Fig. 1(b). It is composed of two inverting gain stages formed by transistors M_{n_1}, M_{p_1} and M_{n_2}, M_{p_2}, respectively. Each gain stage is preceeded by a buffering stage which helps to adapt the DC voltage level at the input of the amplifier. The inverting gain stages are designed to operate in the strong inversion regime, providing a total gain

$$G = \sqrt{\frac{\beta_n\left(\frac{W}{L}\right)_{n_1}}{\beta_p\left(\frac{W}{L}\right)_{p_1}}}\sqrt{\frac{\beta_n\left(\frac{W}{L}\right)_{n_2}}{\beta_p\left(\frac{W}{L}\right)_{p_2}}} \qquad (5)$$

The preamplifying stage was designed to provide a total voltage gain approximately equal to 25.

The transistors aspect ratios $\left(\frac{W}{L}\right)_{n_1} = \frac{2.4\mu m}{2.4\mu m}$, $\left(\frac{W}{L}\right)_{p_1} = \frac{1.2\mu m}{16\mu m}$, $\left(\frac{W}{L}\right)_{n_2} = \frac{1.2\mu m}{1.2\mu m}$, $\left(\frac{W}{L}\right)_{p_2} = \frac{0.6\mu m}{8\mu m}$ were designed to operate in strong inversion while at same time having a moderate current biasing in the order of 1μA per pixel. The first stage is designed with larger transistors as its mismatch is amplified by the voltage gain of the second stage.

In weak inversion the gain of the preamplifying stage becomes

$$G = \left(\frac{n_p}{n_n}\right)^2, \qquad (6)$$

where n_p and n_n are the subthreshold slope factors [16] of the PMOS and NMOS transistors respectively. Thus, the gain of the preamplifying stage would be reduced approximately to 1, if biased in weak inversion.

Voltages V_{adc_1} and V_{adc_2} adapt dynamically to global illumination changes, so that global illumination can change over several decades while the preamplifier stages remain properly biased.

The next stage is a self-clocked switched capacitor differencing and amplification stage as used by Lichtsteiner et al. [9]. Lichtsteiner used a gain of 20 for this stage, which required a C_1/C_2 capacitor ratio of 20, resulting in a high capacitor area consumption. Actually, most of the pixel area (almost 50%) was consumed by these two capacitors. In our case, since we introduce extra gain through the preamplifiers,

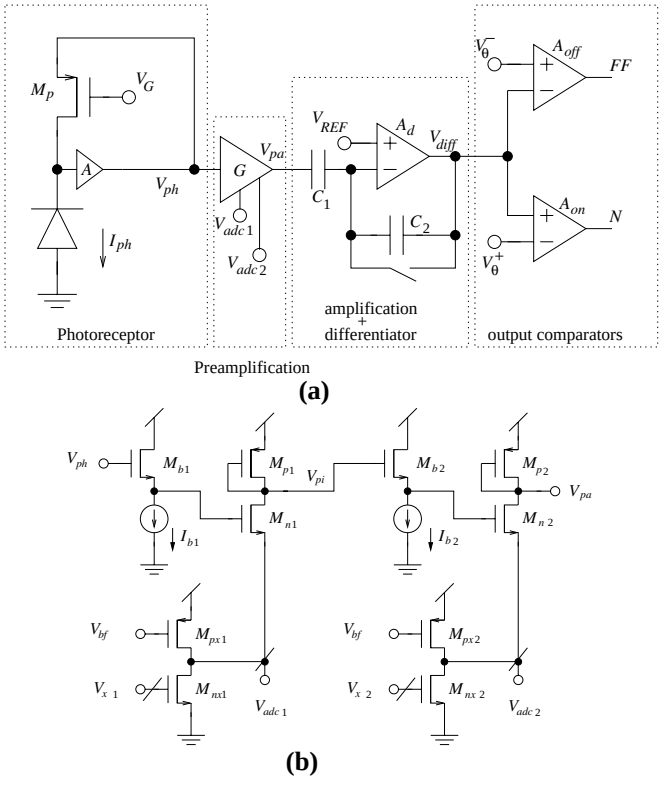


Fig. 1. (a) Block diagram of the pixel and, (b) detailed schematic of the new preamplification block

	This work	Lichtsteiner et al.	Gottardi et al.	Chi et al.	Zaghloul et al.	Gruev et al.	Posch et al. [12]
Resolution	128x128	128x128	128x64	90x90	96x60	189x182	304x240
Fill factor	8.7%	8.1%	20%	17%	14%	30%	10%-20%
Latency	3.6µs	15µs	250µs	<5ms	-	20ms	3µs
Consumption	132-231mW	24mW	100µW	4.3mW	63mW	30mW@5V	50mW-175mW
Technology	0.35µm 4M 2P	0.35µm 4M 2P	0.35µm	0.5µm 3M 2P	0.35µm 4M 2P	0.5µm	0.18µm 4M 2P MIM
Pixel area	35x35µm^2	40x40µm^2	26x26µm^2	25x25µm^2	34x40µm^2	25x25µm^2	20x20µm^2
Chip area	5.5x5.6mm^2	6x6.3mm^2	4.5x2.5mm^2	3x3mm^2	3.5x3.3mm^2	-	9.9x8.2mm^2
Contrast Sensitivity	10%	15%	10%	2.2%	-	-	13% (single pixel)
FPN	4.0% contrast	2.1% contrast	-	0.5% of scale	1-2 decades	0.6% of scale	-
DR	>100dB	120dB	100dB	51dB	50dB	-	125dB
Intrascene DR	56dB	120dB	100dB	51dB		-	125dB

Table 1. Main design specifications and comparison with previous designs

we only implemented a gain of 5 for the switched capacitor differential stage, thus helping to reduce the overall pixel area. If the CMOS process offers the possibility of using MiM capacitors, Lichsteiner's design would be much more area efficient. However, even in this case, introducing these small area pre-amplifiers improves the gain (and therefore the contrast sensitivity) by an extra multiplicative factor.

For the voltage comparators and the in-pixel AER communication circuits, we used the same circuit already reported by Serrano et al. [18].

The complete system architecture block diagram is shown in Fig. 2. The system is composed of a 128x128 pixel array, a row of 128 preamplifier biasing cells that detect the average illumination along that row which adapts the DC levels of the preamplifiers voltage biases V_{adc_1} and V_{adc_2}, a set of programmable current sources that allow to fine tune all the current biases needed by the pixel by accessing to a very reduced set of pins [19], and finally the row and column address event communication circuitry that generates the output addresses. The AER read-out scheme implemented in this design is Boahen's row parallel technique which latches all the events generated simultaneously in a row and reads them out sequentially speeding up significantly the read out process when high event rates have to be managed [20].

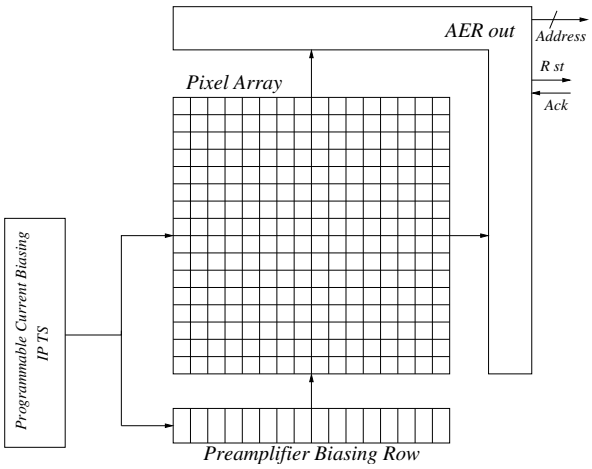


Fig. 2. System block diagram

III. EXPERIMENTAL RESULTS

A prototype has been fabricated in a double-poly 4-metal 0.35µm CMOS technology. The fabricated retina has a resolution of 128x128 pixels and occupies a total area of 5.5x5.7mm^2 including the pads. Fig. 3 shows a microphotograph of the fabricated prototype and Table 1 summarizes the main design specifications [21] and compares them with previously reported designs. The retina was tested with a 16mm F/1.4 C-mount lens. Comparing with the design reported by Lichtsteiner et al. [9], this prototype achieves a lower contrast threshold with a 1/3 area reduction. The latency time has also been reduced from 15µs down to 3.6µs. The current consumption increases due to the preamplification stages. FPN also increases slightly but it remains significantly lower than the achieved contrast sensitivity. The retina achieves a dynamic range higher than 100dB. However, intrascene dynamic range is reduced to a factor of 54dB. Sample images are shown in Fig. 4. Fig. 4(a) and (b) show sample images obtained by histogramming

events over a 40ms period. However, Fig. 4(c) shows an image obtained from a scene where playing cards are passing at high speed. In this case to reproduce a passing card the image has been obtained by histogramming the events captured during a 1.2ms period.

A. Uniformity of Response, Minimum detectable contrast, and Pixel Gain Characterization.

To characterize the uniformity of the response to a given contrast, a similar procedure to the one developed by Lichtsteiner and Delbrück [9] was followed. In order to stimulate all pixels uniformly, a moving gradient bar (shown in Fig. 5(b)) was presented to the retina and the number of positive and negative events generated by each pixel was recorded. The bar crossed the screen in about 4s. For this we used a TFT monitor providing a scene illumination of about 250 lux. The contrast of the stimulus was measured to be $\theta = \ln(I_{bright}/I_{dark}) = 1.39$ (which corresponds to a 1:4 contrast, or 400%). The experiment was repeated for different settings of the pixel thresholds. The bar was swept 30 times for each setting. This way, for each pixel (x, y) we obtain its corresponding number of positive $N^{+}(x, y)$ and negative $N^{-}(x, y)$ events fired per edge presentation for the different settings of threshold voltages ($\left|V_{REF} - V_{\theta}^{+/-}\right|$). The number of events generated by a pixel for a given stimulus contrast θ and threshold voltage setting is given by

$$N^{+/-} = \theta/\theta_{ev}^{+/-} \tag{7}$$

Consequently, for each pixel we can compute its contrast sensitivity $\hat{\theta}_{ev}^{+/-}(x, y) = \theta/N^{+/-}(x, y)$, and generate the corresponding histogram for $\theta_{ev}^{+/-}$ as shown in Fig. 5(a). As can be observed, it was possible to set an average contrast threshold as low as $\theta_{ev} = 10.45\%$ with a FPN of $\sigma(\theta_{ev}) = 4.0\%$. It was possible to adjust a lower threshold value, but then the output was dominated by noise events.

Using eq. (4) and the measured mean values of the contrast thresholds θ_{ev}^{+} and θ_{ev}^{-} we can estimate the achieved

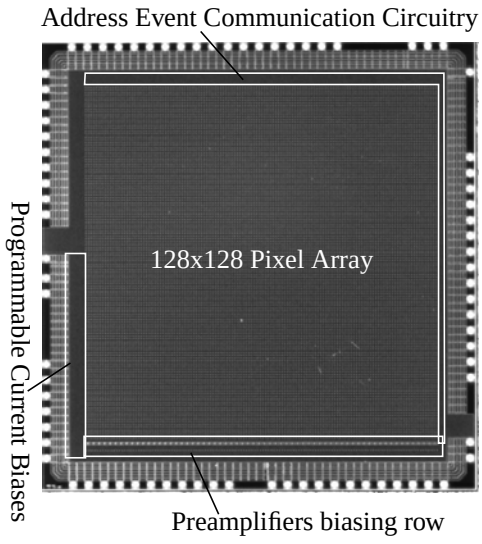


Fig. 3. Microphotograph of the fabricated prototype with specification of the area dedicated to the main blocks

(a)

(b)

(c)

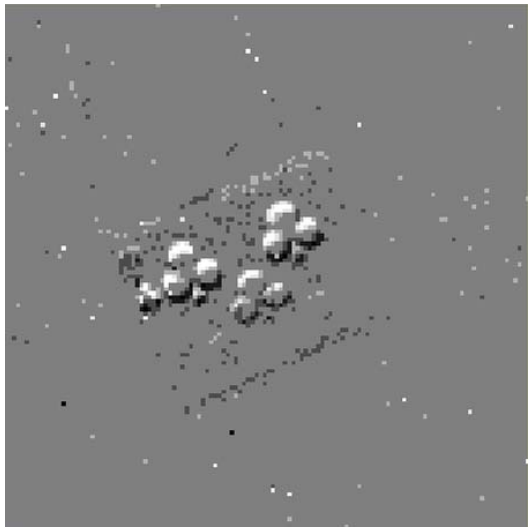


Fig. 4. (a) and (b) Sample images created by histogramming events over a 40ms period, and (c) Sample image created by histogramming events over a 1.2ms period.

value of the average pixel gain $\bar{A}$. By representing the average contrast threshold (θ^{+}_{ev} and θ^{-}_{ev}) as a function of the voltage threshold $\left|V_{REF} - V_{\theta}^{+/-}\right|$, and fitting these graphs to straight lines, we can obtain the average gain $\bar{A}$ from the slopes, as well as the average offset voltages for $\overline{V_{os} + V_{osn}}$ and $\overline{V_{os} - V_{osf}}$. The resulting average gain is $\bar{A} = 60.8$, while the offsets are $\overline{V_{os} + V_{osn}} = 103mV$ and $\overline{V_{os} - V_{osf}} = 89mV$. Assuming $\overline{V_{osn}} = \overline{V_{osf}}$ results in $\overline{V_{osn}} = \overline{V_{osf}} = 7mV$ and $\overline{V_{os}} = 96mV$. This latter offset is dominated by reset switching induced offset.

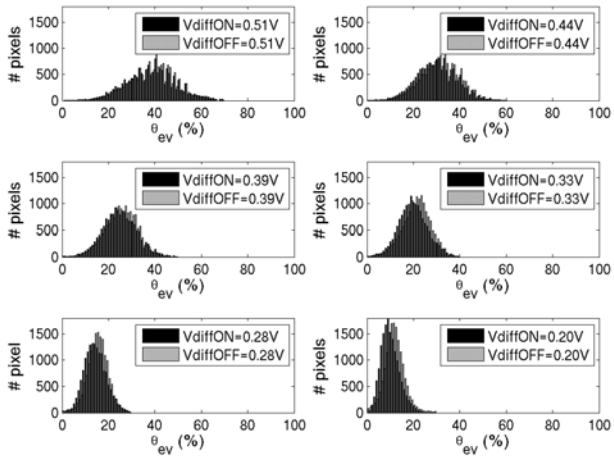
B. Dynamic Range

The operation of the retina has been verified for over 100dBs of illumination change. The retina has been tested for bright illumination (higher than 50Klux) down to illuminations below 1lux. The lower illumination limit of the retina is limited by the dark current of the photodiodes which is lower than 12fA.

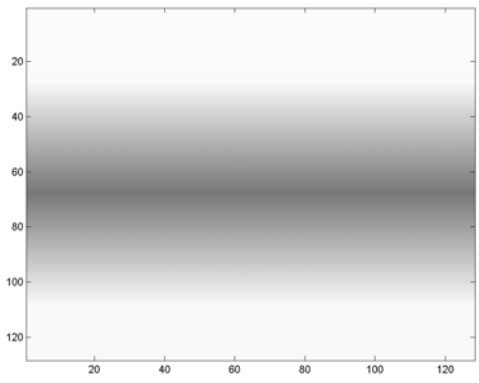
Intra-scene illumination range of the retina is limited, since the preamplifying stage self-adapts to one single global illumination level. Nevertheless, an intra-scene illumination dynamic range of up to 54dB has been verified.

C. Pixel Bandwidth

To measure the pixel bandwidth a group of pixels located in the center of the array were stimulated with a flashing



(a)



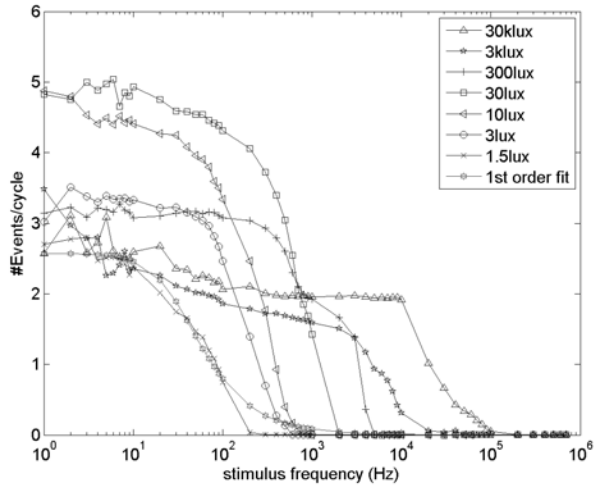
(b)

Fig. 5. (a) Histogram of the pixel contrast threshold for different settings of the comparator voltages, and (b) applied stimulus

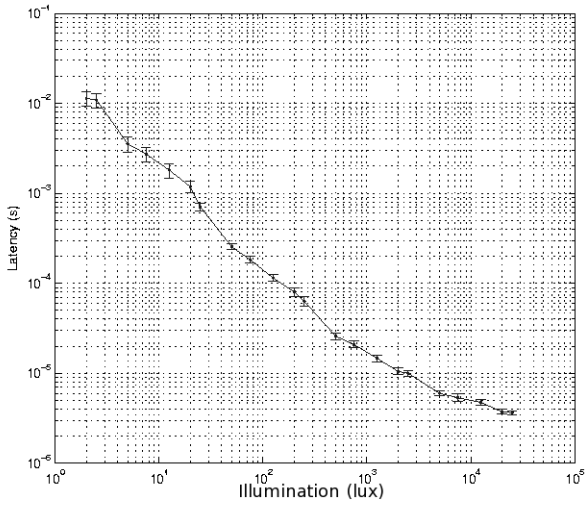
Kingbright super bright red LED L-793SRC-B (1400mcd@20mA) following a similar procedure as the one developed by Lichtsteiner and Delbruck [9]. We created a scene illumination by placing two CFL bulbs near the retina but not directly focused on it. A scene illumination of 30klux was measured by placing the light meter RS-180-7133 in the retina position. The LED was placed in front of the retina. The LED diode was modulated with a sinusoidal signal

$$V(t) = V_{off} + A\sin 2\pi ft \tag{8}$$

We varied the frequency of the sinusoid and counted the number of positive and negative events generated by each stimulated pixel per period of the sinewave. The measurements were averaged over a 20 seconds time period. If the magnitude of the stimulus contrast and the voltage thresholds are kept constant, the pixel gain is directly related to the number of generated events (see eqs. (4) and (7)). The measurements were repeated for different values of the illumination by inserting neutral density filters of different attenuation values. Fig. 7(a) plots the measured values of the events per cycle as a function of the frequency of the



(a)



(b)

Fig. 6. (a) Measured bandwith for different illumination values, and (b) measured latency as a function of the illumination

sinusoidal signal for different illumination values. As can be observed, for intense illuminations in the order of 30Klux the sensor bandwith is about 10KHz. This makes this sensor specially appropriate for very fast moving objects. According to our measurements the sensor can detect moving objects at frequencies higher than 10KHz.

D. Latency

Latency is the delay it takes from the occurrence of an illumination change at the photodiode until the corresponding output event is transmitted off-chip. To measure the latency, we used the same setting than in the previous bandwith measurements, the super bright LED with the two CLF bulbs placed near the retina to create an intense scene ilumination, but now the LED was stimulated with a step signal [9]. We measured the latency as the delay between the step in the LED signal and the first output request corresponding to an event with the address of the stimulated pixel. We performed the measurements for different values of the illumination by inserting neutral density filters in front of the retina. Each measurement was repeated a total of 30 times. The results of these measurements are shown in Fig. 7(b) which plots the measured latency as a function of the illumination. The latency deviation measured among the 30 trials is also marked with error bars. As can be observed, the latency is inversely proportional to the illumination. For very low illumination (in the order of 1 lux) the measured latency is $10ms$, while for high level of illumination (10 Klux) the measured latency was 3.6µs.

E. Power Consumption

Chip power consumption has been characterized. The total current consumption includes the current consumed by the programmable current biasing block, the pixel analog and digital parts, and the peripheral AER communication circuitry. At low output event rates the current consumption is dominated by the analog parts, which depends on the chip biasing, while at high event rates the current is consumed mainly by the digital event generation parts. The current consumption at moderate output event rates (below 1*Meps*) is approximately 44mA from a 3.3V power supply, that is a consumption of 145mW. Most of this current consumption comes from the strong inversion biased preamplifier stages. For very high event rates (above 1*Meps*) there is a sudden increase in power consumption because now the contribution of the digital output pads (and all the AER communication circuitry) becomes larger than that of the preamplifier stages.

IV. CONCLUSIONS

A 128x128 temporal contrast retina has been implemented. The new design including a low area preamplifying stage allows to improve contrast sensitivity over previous designs while reducing the pixel area by a 1/3 factor. Designing preamplifying stages operating at low currents to reduce static power consumption is an objective of future work.

V. ACKNOWLEDGEMENTS

This work has been supported by EU grant FP7-ICT-2007-1-216777 (NABAB), Spanish research grants (with support from the European Regional Development Fund) TEC2006-11730-C03-01 (SAMANTA2), TEC2009-10639-C04-01 (VULCANO), and Andalusian research project P06-TIC-1417 (Brain System). JALB was supported by the JAE program of the Spanish Research Council.

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