Trabajo Fin de Máster
"Máster Universitario en Microelectrónica: Diseño y Aplicaciones de Sistemas Micro/Nanométricos"

Safety Acquisition System for Graphene Based Transistors

Lucía-Jésica Ré Blanco

Juan Antonio Leñero Bardallo (US)

Anton Guimerà Brunet (IMB-CNM, CSIC)

06/2020

Index

1 Motivation and Objectives

Recently, the use of active transducers based on graphene transistors (gSGFETs) for recording neural activity have demonstrated several advantages compared with commonly used technologies based on metal electrodes. One of these advantages is the unique ability for recording very low frequency signals, which could improve the understanding of certain neurological diseases such as epilepsy, migraine or brain stroke, and improve its diagnostic and treatment. However, the use of these technology is limited to experimental electrophysiology due to the lack of acquisition electronics compatible with the electric safety regulatory. The main limitation to meet with the regulatory requirements come from the need of a DC coupling operation to fix the optimal bias point, which means that the system is unable to limit leakage current through a patient in case of failure. Therefore, the main goal in this master thesis is to design an acquisition system that meets with the regulatory aspects applicable to medical devices, enabling the use of this technology in human clinical trials. This objective has been divided in the following sub-objectives:

- To evaluate the electrical safety regulatory applicable to electrical medical equipment.
- To design and develop an electronic system for acquiring neural signals using graphene transistors able to limit the current leakage through a patient.
- To validate the recording capabilities of the developed system.

The work presented in this master thesis has been developed in the framework of the project GrapheneCore2 (785219) FETFlagship EU-H2020 funded by the European Commission.

2 Introduction

2.1 Graphene

Graphene is a nanometric, two-dimensional material that is composed of a single layer of carbon atoms conforming a honeycomb shaped network. Graphene is the basic building block to form different allotropes such as 3D graphite or one-dimensional carbon nanotubes obtained by stacking or rolling graphene sheets (figure 1a).

Graphene has extraordinary electrical, thermal and mechanical properties thanks to its electrical band structure [1]. The band structure (figure 1b) shows multiple symmetries at the κ points at the corners of the graphene Brillouin zone [2], those points are called Dirac points. On those places valence and conduction bands are in contact, which means that graphene is a zero-gap semiconductor. This fact allows Fermi level to shift between conduction and valence bands directly, making graphene a material that can act as 'n' or 'p' type semiconductor.

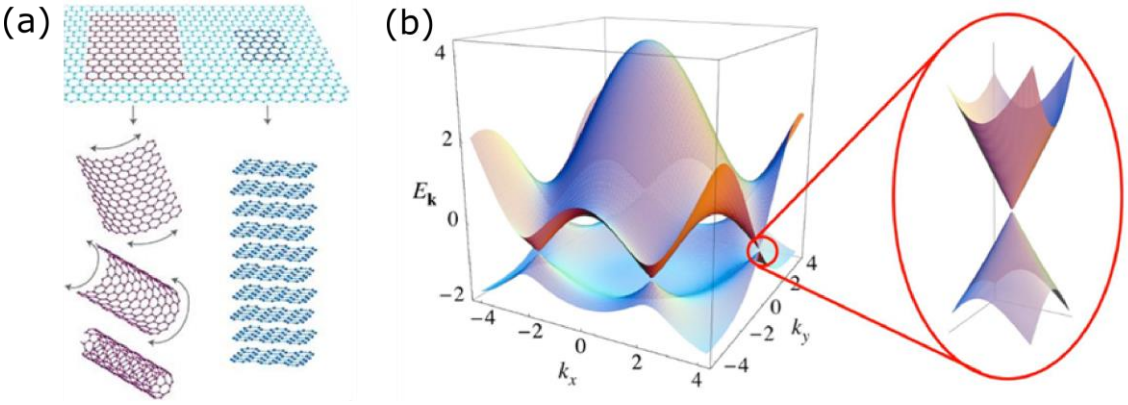

Figure 1 a) Graphene sheet and its use as basic building block to nanotubes and stacking. b) Three dimensional plot of graphene band structure. At the zoom area the zero-gap between valence and conducting band can be seen

Graphene shows a high mobility of its electrons with a theoretical limit of 200.000cm^2/(V·s), which is more than 100 times higher than silicon electrons mobility. It also has a huge thermic and electric conductivity thanks to its atomic distribution that allows free electrons to move avoiding collisions between them and atoms and decreasing Joule effect. Graphene shows a 10 times better thermic conductivity than copper and much more electric conductivity than silicon.

Moreover, it is a chemically stable material thanks to the fact that all its p_z atomic orbitals are strongly coupled and stabilized in a delocalized π bonding system (figure 2). This

property allows graphene to avoid chemical reactions such as hydrolysis or oxidation [3] [4] produced by biochemical factors such as pH, heat, light, humidity, enzymes or oxygen, being a biocompatible material [5]. The wide electrochemical window in aqueous environments [6] enables the use in medical applications such as neural interfaces, being a good candidate to be used as a transducer between the neural tissue and the electronic recording systems.

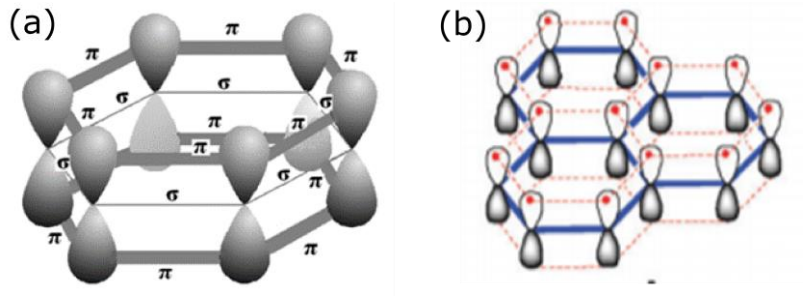

Figure 2 a) π and σ bonding representation of a honeycomb shaped system. B) P_z orbitals of graphene in a delocalized π-bonding system. Dashed lines indicate the overlap between p_z orbitals

Lastly, is also important to mention that graphene is an elastic and flexible material thanks to its thinness. These properties are very important for the use of graphene in electrophysiological applications, allowing a better attachment between the recording device and the curved and textured surface of the brain [7]. This thinness of graphene also results in a low optical absorption of only 2.3% [8] in the visible range, appearing such a transparent material. This allows the use of graphene in optogenetics, a biological technique that involves the use of light to control neurons ion channels that are light-sensitive.

2.2 Solution-Gated Field-effect transistors

2.2.1 Basic Concepts

A standard MOSFET (figure 3a) is composed of two doped zones with terminals over a silicon substrate, forming the source and the drain, and a silicon dioxide layer covered with a metal that implements the gate. When a gate potential is applied, a conducting channel is induced in the silicon, which can be interpreted as a resistor between source and drain.

Metal gate of MOSFET can be changed by an electrolyte solution (fig 3b). When the MOS is immersed, a double layer is formed at the solution-oxide interface. If the oxide

thickness is small enough, this double layer interacts with the double layer generated at the oxide-silicon junction, so the induced conducting channel in the silicon depends on the ion activity in the solution where MOS is immersed. If the ion charge changes, the channel conductivity also does. This three terminal transistor based on MOSFET configuration is called SGFET and was developed by Bergveld in 1970 [9].

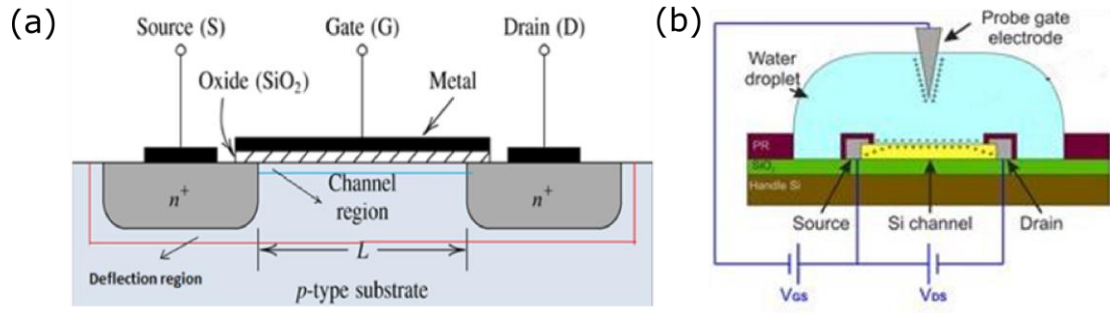

Figure 3 a) Standard MOSFET configuration with two doped zones (D and S) and a SiO_2 layer covered with metal (G). b) SGET configuration formed immersing a MOS without gate metal in a water droplet. Gate-source polarization is applied on the gate using a probe gate electrode. Figure adapted from [10]

In the case of graphene based solution gated field effect transistors (gSGFETs) (figure 4) the graphene is used as a semimetal channel material, and its conductivity is modulated through the potential applied between the electrolyte solution and the graphene. Thanks to its wide electrochemical window, it can be implemented without any dielectric layer between the graphene and the electrolyte solution. Thus, increasing the gate capacitance in one order of magnitude compared with SGFETs based on standard semiconductors, having been reported values about $2\mu F \cdot cm^{-2}$. This higher value of input capacitance results in a very high transconductance and also in a higher sensitivity of the devices to gate potential changes. High transconductance values also allows to use drain-to-source voltage below 100mV resulting in a low power consumption. This, being useful for its application in chronic studies where an external battery supplies the devices.

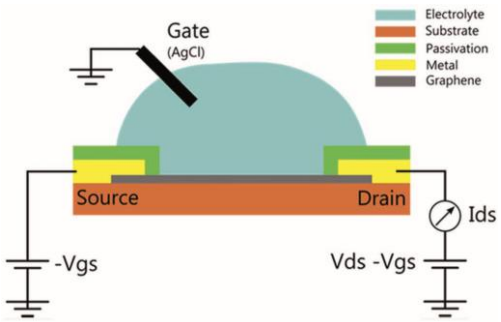

Figure 4 Cross-section of gSGFET device using an electrolyte as aqueous medium. Gate-source polarization is applied on the gate using an AgCl reference and drain-source polarization is applied on the drain. Figure adapted from [10]

In figure 5 an energy band diagram of the graphene-electrolyte interface is shown to explain the modulation of the channel conductivity when Vgs changes. When a voltage is applied between the gate electrode and the graphene, graphene's Fermi level shifts so the number of free carriers in graphene changes. The valence and the conduction band meet at the Dirac point (when the conductivity is minimum). The gate potential at which Dirac point is reached is called Charge Neutrality Point (CNP) and depends on many factors such as the doping level of graphene sheet, the electrolyte solution or the electrochemical potential of the reference electrode. Due to the fact that graphene transistors are ambipolar devices, depending on the Fermi level respect to CNP the channel will transport mostly holes or electrons.

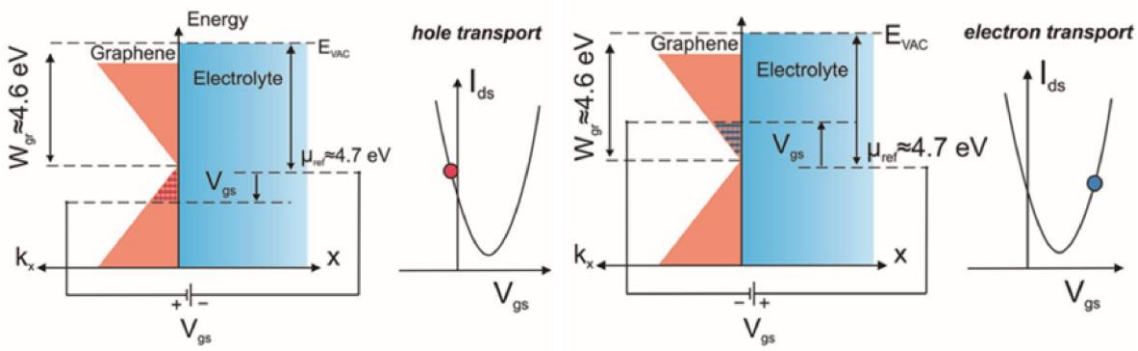

Figure 5 Figure adapted from [10].Basic momentum-energy diagrams of the graphene-electrolyte itnerface when using Ag/AgCl reference electrode (with an electrochemical potential μ_{ref} around 4.7eV) showing a work function of the graphene around 4.6eV. The related Drain-Source current (I_{ds}) respect with the voltage gate (V_{gs}) are shown.

Graphene based solution-gated field-effect transistors (gSGFETs) are investigated to implement efficient transducers for neural electrical signals. As explained, the high chemical stability of graphene allows transistors to work without a gate dielectric layer, as a consequence, the gate capacitance and the transistor transconductance are increased. Also, the mechanical conformability of graphene enables the design of neural interfaces conformable to the brain surface, and the optical transparency of a single layer of graphene enables the possibility of combining electrical neural recordings with the optogenetics techniques.

gSGFET configuration reduces the sensitivity to external noise sources thanks to its intrinsic local amplification, and the use of transistors as transducers, also enables multiplexing strategies implementation [11], allowing the reduction of connectivity and scaling up the number of recording sites. The transconductance of gSGFETs is stable even at very low frequencies, allowing DC coupled operation.

This technology overcome high common voltage limitations of passive electrodes in DC coupled operation, and also voltage drifts. Furthermore, signal attenuation produced by the voltage divider between the electrode impedance and the input impedance amplifier [12], is avoid thanks to the fact that the electrode-electrolyte interface capacitance of gSGFETs is part of the device and the input capacitance for the signal.

2.2.2 Fabrication of gSGFET

gSGFETs fabrication has been performed in the clean-room facilities located in the *Institut de Microeletrònica de Barcelona - Centro Nacional de Microelectrónica* (IMB-CNM). The main challenge lies in the incorporation of graphene into standard microelectronic processes. This is achieved with a fabrication protocol that also permits the making of devices into polyamide. The process flow used is shown in figure 6.

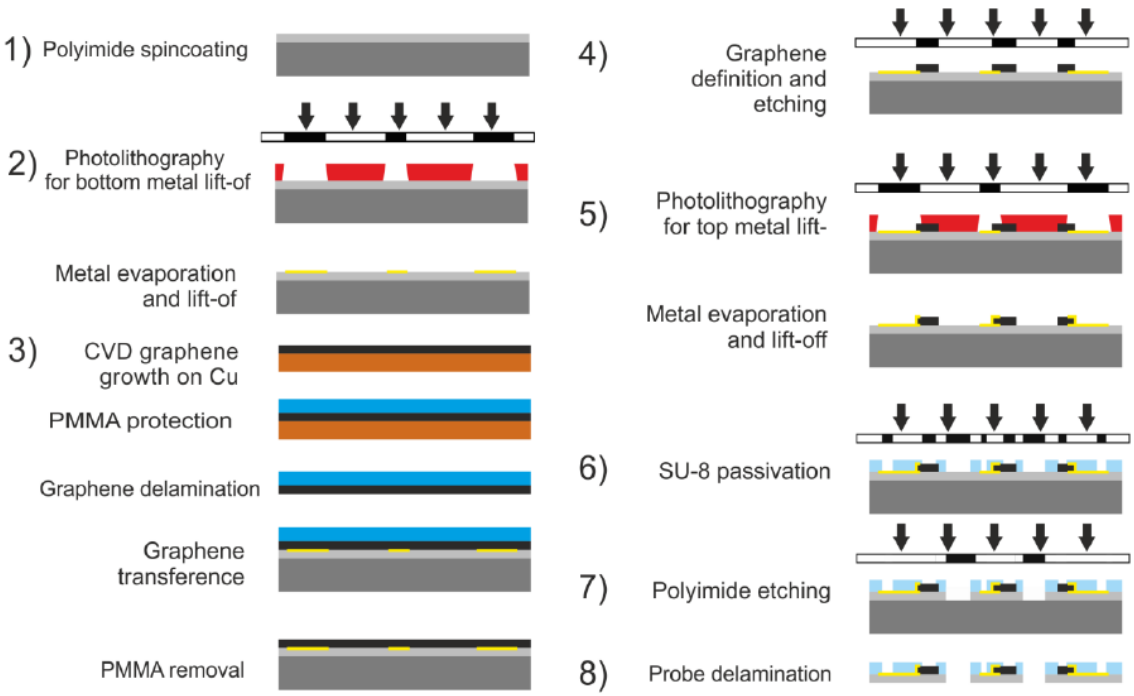

Figure 6 Process flow of the gSGFETs fabrication over flexible polyamide substrate. Figure adapted from [13]

2.2.3 Characterization of gSGFET

To electrically characterize the transistors, a matrix of transistors (figure 7) is connected to a PCB using a Zero Insertion Force (ZIF) connector. The probe is immersed in phosphate buffered saline (PBS) and an Ag/AgCl electrode is used as reference.

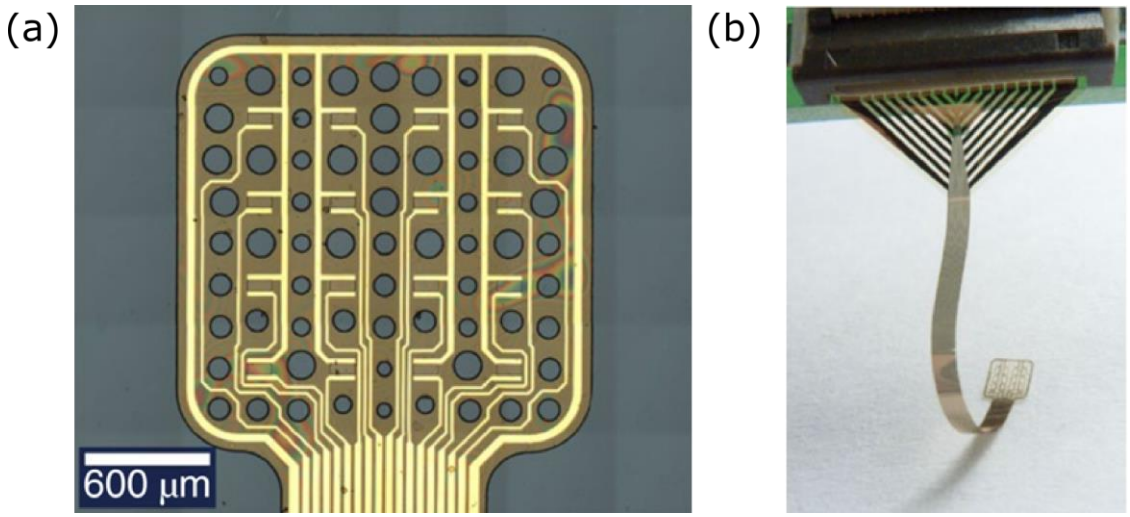

Figure 7 a) Optical microscope image of the active area of a 4x4 gSGFET array. b) Photograph of the neural probe after peeling from the water and being introduced into a ZIF connector.

The basic electrical characterization of sGFETs consist in measure its transfer curve (I-V characteristic) and evaluate its intrinsic noise. To do this, the I_{ds} current is recorded and the power spectral density (PSD) is calculated for each bias point. Combining both characterizations some parameters can be obtained:

- Resistance (R): ideally, corresponds to the graphene channel resistance. In the real scenario, other series resistances such as the track resistance and the contact (resistance between the graphene and the metal tracks) can also contribute to this parameter.

$$R_{ds} = \frac{V_{ds}}{I_{ds}} \tag{1}$$

- Transconductance (gm): is the variation of the drain current respect to the gate voltage. It is proportional to the graphene sheet mobility and gate capacitance and indicates the sensitivity of the device to gate potential changes. Usually, it is normalized by the V_{ds} applied.

$$g_m = \frac{dI_D}{dV_{GS}}\Big|_{V_{DS}} \tag{2}$$

- Dirac Point (U_D): refers to the gate voltage at which the minimum drain current is obtained. It depends on the doping level of the graphene sheet used as channel of the devices but also, on the electrolyte solution and the electrochemical potential of the reference electrode used for the characterization. Its value is calculated as:

$$U_D \approx U_{D0} + \frac{V_{DS}}{2} \quad (3)$$

Where U_{D0} is the theoretical voltage when drain voltage is not applied. It can be calculated, if it there is no doping, as:

$$U_{D0} = \frac{E_F}{q} \quad (4)$$

Where E_F corresponds to the difference between graphene work function [14] (e.g. 4.6eV) and the electrochemical potential of the reference electrode (e.g. 4.7eV).

- Noise: The PSD shows the typical 1/f shape of these devices. Integrating the PSD in a bandwidth the I_{RMS} is obtained, which is the current noise measured at the drain of the transistors. V_{RMS} [15] is calculated dividing I_{RMS} by the transconducntance of the device. This parameter indicates equivalent the noise at the gate of the transistor, thus being very important for the recording applications of gSGFETs because it indicates the minimum amplitude signal that can be detected.

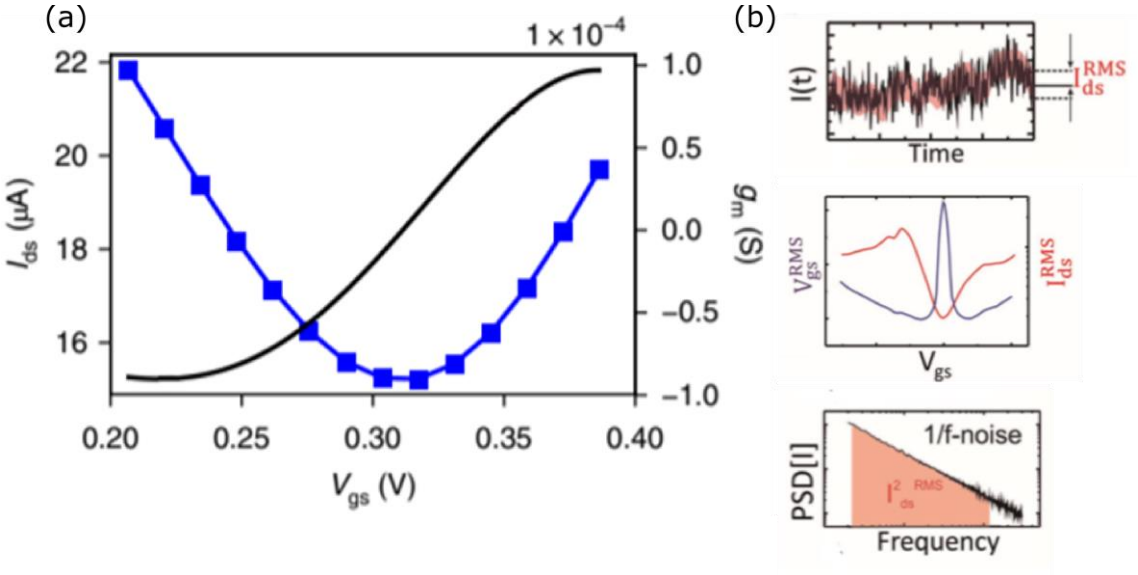

Figure 8 DC characterization of a 100x50 μm² gSGFET in 10mM PBS with drain-source voltage bias of 50mV. a) gSGFET drain-source current (I_{ds}) vs gate-source voltage (V_{gs}) (blue line) and transconductance (g_m) obtained as the first derivative (black line). b) Measurement of the current fluctuation (I(t)), related RMS current and voltage noise (I_{rms} and V_{rms}) for different gate biases and calculation of the PSD.

2.3 International Standard IEC60601-1 for Medical electrical equipment

IEC60601-1 [16] is the standard in which regulations related to the safety of medical equipment are grouped and is part of IEC60601 published for the first time in 1977.

A Medical electric equipment is an electrical equipment designed for treatment, monitoring or diagnose of patients, powered from one connection to main supply. There are two classes for this equipment:

- Class I: use single insulation protecting against electric shock by a protective Ground.
- Class II: use double insulation, designed in such a way that is still safe in case of ground connection failure.

Often, patients are physically connected to electrical medical devices so they are exposed to electrical currents that can travel through the human body causing problems in the respiratory system, in the heart or in the brain. If the medical electric equipment is designed to come into physical contact with the patient, the part in contact is called applied part, these can be:

- F-type: electrically isolated from Ground and other parts of the medical equipment. These parts are either type BF or CF.
- Type B: parts ground referenced that are not suitable for their use in direct contact with the heart.
- Type BF: F-type applied part that complies with a high degree of protection against electric shock than type B.
- Type CF: F-type applied part complying the highest degree of protection against electric shock.

Type CF applied parts are suitable for direct cardiac application, and as it is the most restrictive type, it is suitable for brain application.

One of the most important restrictions in the standard is about the leakage current. This current is often the source of injury or death. When electrical current flows through a human body the effect depends on the amount of current and on the amount of time the current is flowing.

The standard defines three different sources of leakage current:

- Ground leakage: current flowing down the protective ground conductor.
- Enclosure leakage: current flows to ground through a person by touching the medical equipment or part of it.
- Patient leakage: current flowing through a person to Ground from an applied part, applying unintended voltage from an external source.

For patient leakage tests [17] IEC 60601-1 specifies that the measurements must be done under normal and reverse operation of the main supply and single fault conditions, open neutral circuit and open Ground. The regulation also specifies that for CF-Type applied parts, the leakage current has to be measured from each of the patient's connection separately while for B and BF-Type leakage current is measured with all parts of the same type connected together.

Diagram of figure 9 shows the schematic of the circuit used to perform patient leakage measurement, including the relays to force single fault conditions:

- Normal Condition: measurement of patient leakage current under normal conditions. S1 and S8 are closed and S5 is set normal and then reversed.
- SFC – Supply Open: measurement of patient leakage current when Main Supply is open. S1 is open, S8 is closed and S5 is set normal and then reversed.
- SFC – Ground Open: measurement of patient leakage current when Ground is open. S1 is closed, S8 is opened and S5 is set normal and then reversed.

As F-type parts need to ensure a high degree of protection against electric shock, F-type patient leakage test has to be also performed to guarantee the accomplishment of leakage regulations applying 110% of the main input voltage to the applied part connections. Diagram of figure 10 shows the test circuit for this type of test. In this test current is measured with S1 and S8 closed while S5 and S9 are switched between normal and reversed.

With all the measurements and tests being taken into account, standard IEC 60601-1 defines the current limits for each type of applied parts and current type (figure 11).

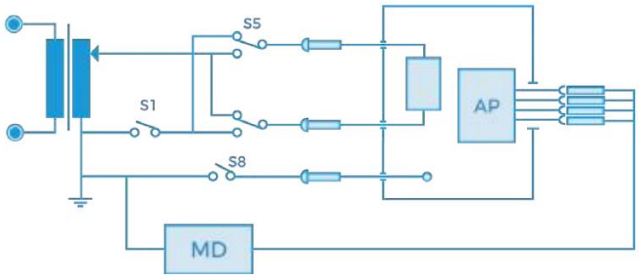

Figure 9 Test circuit for patient leakage current. Main Supply (transformer) is connected, using the different relay's configuration, to the Applied Part (AP). Leakage current is measured with the MD (Measurement Device)

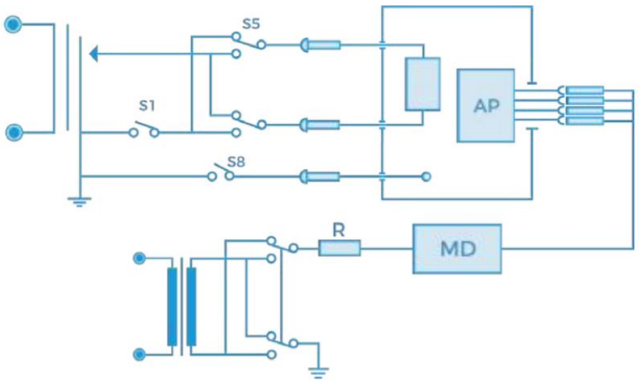

Figure 10 Test circuit for patient leakage current for F-Type applied parts. As its needed to achieve 110% of main supply voltage there are two connections to the applied part, once through S5 Relay and the other through S9 relay and MD (Measuring Device). This tests is hazardous to the user so a resistor (R) is put in series with MD to achieve a limit current.

In this Master Thesis it is wanted to use gSGFETs transistors as applied parts in direct contact with human brain to be able of recording real time signals to obtain information about brain diseases behaviour. The system used to perform the acquisition of this data must be design accomplishing IEC60601-1 regulation for F-type applied parts. Patient leakage and F-type patient leakage test have to be successfully passed by the electrical medical device considering the most restrictive limitations, namely, CF- type applied part ones. Summarizing, the designed acquisition system has to avoid that more than 10µA and 50µA of DC current go through a patient in normal and single fault conditions respectively.

	Type B applied parts		Type BF applied parts		Type CF applied parts	
Leakage current type	**NC**	**SFC**	**NC**	**SFC**	**NC**	**SFC**
Ground leakage (4th edition)*	5000µA	10000µA	5000µA	10000µA	5000µA	10000µA
Ground leakage (General)	500µA	1000µA	500µA	1000µA	500µA	1000µA
Enclosure leakage	0.1mA	0.5mA	0.1mA	0.5mA	0.1mA	0.5mA
Patient leakage (dc)	100µA	500µA	100µA	500µA	10µA	50µA
Patient leakage (ac)	100µA	500µA	100µA	500µA	10µA	50µA
Patient leakage (F-Type)	NA	NA	NA	5000µA	NA	50µA
Patient leakage (mains on SIP/SOP)	NA	5000µA	NA	NA	NA	NA
Patient auxiliary current (dc)	10µA	50µA	10µA	50µA	10µA	50µA
Patient auxiliary current (ac)	100µA	500µA	100µA	500µA	10µA	50µA

Figure 11 IEC 60601-1 test limits. CF-Type applied parts Patient Leakage limits (in DC) are marked in red because these values will be the ones taken into account to design gSGFETs electronics to allows its use being in direct brain contact.

3 Neural signal acquisition based on gSGFETs

3.1 Implementation of Leakage Current Limitation

Most of the systems used for recording neural signals are based on electrodes as transducer element [12]. In these systems, neural signal acquisition is based on the amplification of the electrode's voltage, so the acquisition electronic system (figure 12a) basically consists on a voltage amplifier with a high input impedance to avoid a drop voltage due to the electrode impedance.

Unlike these systems, acquisition systems based on active elements needs to perform two functions:

1) To polarize the transducer device at an optimal working point.

2) To amplify the signal proportional to the neural activity recorded by the transducer.

So the acquisition electronic system (figure 12b) is composed of DC voltage sources to correctly polarize the transducer and a transimpedance amplifier that converts the current signal into a voltage signal to be acquired by an ADC converter.

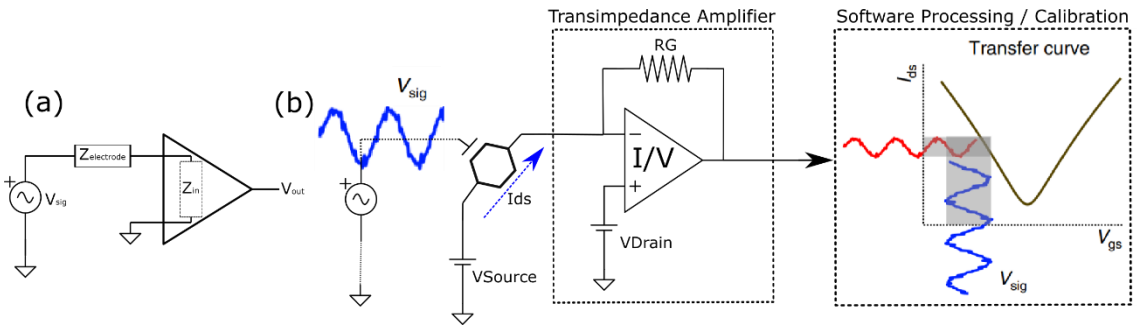

Figure 12 ***a)*** *Schematic of an acquisition system based on electrodes, where the measured voltage is controlled by the effective electrode impedance ($Z_{electrode}$) and the effective input impedance (Z_{in}).* ***b)*** *Schematic of an acquisition system based on active transducer (gSGFET). VDrain and VSource voltage sources fix the bias point and the trans-impedance amplifier converts the transistor current (Ids) into voltage.*

The most used acquisition system based on active transducers requires a DC coupling operation to fix the optimal bias point. This fact limits the compliance with IEC60601-1 regulation applicable to electrical medical equipment, which limits maximum low

frequency (DC) leakage current through a patient, and therefore bans its use in clinical applications. To enable the use of active transducers instead of electrodes in clinical applications and take profit of their advantages, the acquisition system must ensure patient safety if a simple failure occurs. For this reason, it is necessary to define a method to limit the leakage current and at the same time allow the bias point control.

Here, we propose a method which consists on the use of three passive components to connect the transducer element (e.g. *gSGFETs*) to the electronic system (figure 13), together with the use of an AC signal coupling for the acquisition of the neural activity. The passive components ensure the limitation of the leakage current in any case, even in the case of electronics breakdown (IEC60601-1 simple failure scenario). These passive components, limit the leakage currents, but also limit the DC current through the transistor (I_{ds}) which contains the neural signal to be acquired. So, the use of these protective elements requires an AC signal coupling strategy, which moves the neural signal to higher frequencies where the current is not limited.

3.1.1 DC vs AC signal coupling

In an AC signal coupled system the active transducer element (*gSGFETs*) behaves as a signal mixer between a carrier signal and the neural signal, allowing the use of Amplitude Modulation (*AM*) techniques for the signal amplification and processing. Figure 13 shows the placement of the protective passive components, where, R_{DC} limits the maximum leakage current and allows to set the voltage bias point, and Cd/Cs blocks any DC current while allows the pass of AC current which contains the recorded signal.

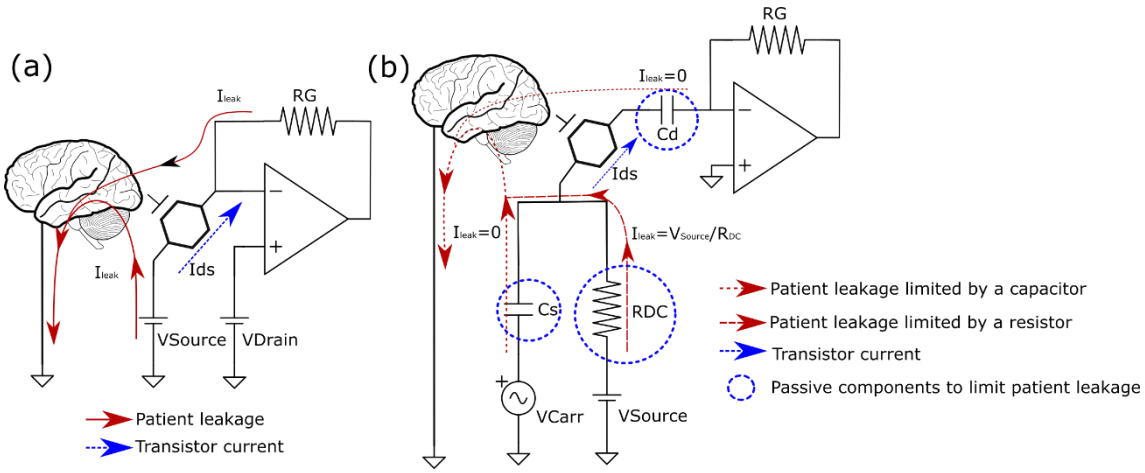

Figure 13 a) DC coupling system . b) AC coupling system. Red arrows indicate the possible leackage current paths. Components rounded with a blue circle are the passive components which limit the leackage current.

3.1.2 AM Modulation and Demodulation

The AM modulation consists on a mixer that multiplies a carrier signal and a modulator signal (figure 14). The carrier wave (f_c) is a high frequency signal whose amplitude will be a function of the modulator signal (f_m).

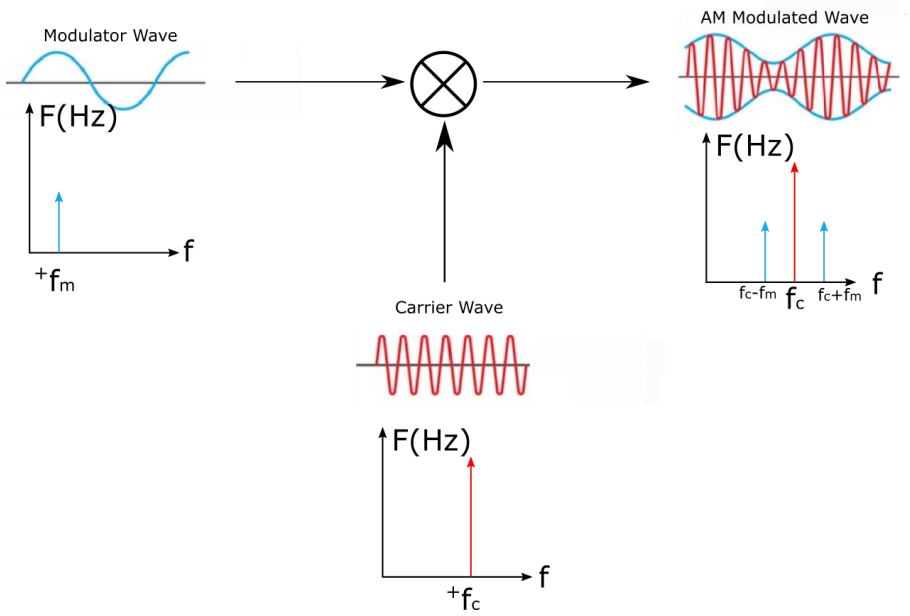

Figure 14 General AM modulation scheme. The Modulator wave of f_m frequency (blue wave) is multiplied with the carrier wave of f_c frequency (red wave) using a mixer. AM Modulated wave frequency spectrum it's centred at f_c (red) and has two side bands of f_c-f_m and f_c+f_m (blue).

The modulator signal can be recovered by a demodulation process which consists on a product detector (figure 15). The input signal is multiplied by a carrier signal produced with a local oscillator to move the signal to the baseband following the expression:

$$v_{AM}(t) = V_c \cdot [1 + v_m(t)] \cdot \cos(w_c t + \varphi_m) \tag{5}$$

$$v_{OL}(t) = V_{OL} \cdot \cos(w_{OL} t + \varphi)$$

$$v_o(t) = \left\{\frac{1}{2} V_c V_{OL} \cdot [1 + v_m(t)]\right\} \cdot \{\cos[(2w_c)t + \varphi_m + \varphi] + \cos[\varphi_m - \varphi]\} \tag{6}$$

Where $v_o(t)$ is the signal obtained after multiplying $v_{AM}(t)$, which is the modulated signal with an amplitude V_c, and $v_{OL}(t)$ is the signal generated by the local oscillator with a V_{OL} amplitude. Finally, $v_m(t)$ is the modulator signal, which is the signal that has to be recovered.

Looking at equation 6 it can be seen that the obtained signal $v_o(t)$ has been moved to baseband but also moved to $2f_c$. For this reason a low pass filter is applied to remove remaining high frequency components and only keep base band information.

$$v_f(t) = \left\{\frac{1}{2}V_c V_{OL} \cdot [1 + v_m(t)]\right\} \tag{7}$$

If the phase of $v_{OL}(t)$ is not null, which often occurs in the real picture, it has to be included a lock-in phase process before the product detector, to compensate the phase difference in the local oscillator. As in this system only one signal is going to be recovered by each product detector, it is possible to avoid the lock-in phase step by multiplying $v_{AM}(t)$ signal by both, cosine and sine of $v_{OL}(t)$. This way, if a phase difference exists, $v_m(t)$ information is distributed into real and imaginary parts, being its absolute value, the entire $v_m(t)$ recovered.

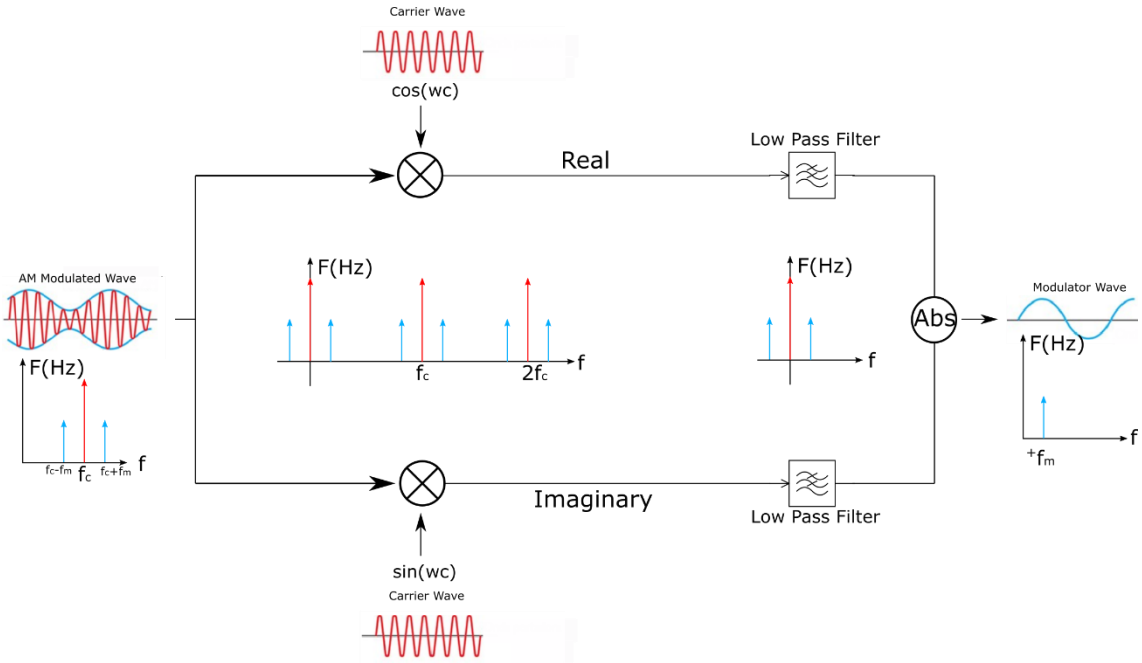

Figure 15 Product detector scheme. AM signal is multiplied with a local carrier signal of frequency w_c with 0º phase (cosinus) to obtain real part and 90º phase (sinus) to obtain imaginary part. A low pass filter is used to eliminate high frequency components and the absolute output value is the original modulated signal of frequency w_m

3.2.2 gSGFET as a mixer

gSGFET can be used as a mixer to implement an AC coupled acquisition system. In this case, an electrical potential fluctuation applied on the gate (i.e neural signal) change the conductivity of the channel through the gate capacitance. Therefore, applying a pure tone

voltage signal on the transistor source (V_{carr}), the current through the channel (I_{ds}) results from the product of $V_{carr}(t)\cdot V_{sig}(t)$ (equation 5) (figure 16), where $V_{sig}(t)$ is the brain signal applied in the gate of the device (V_{gs}).

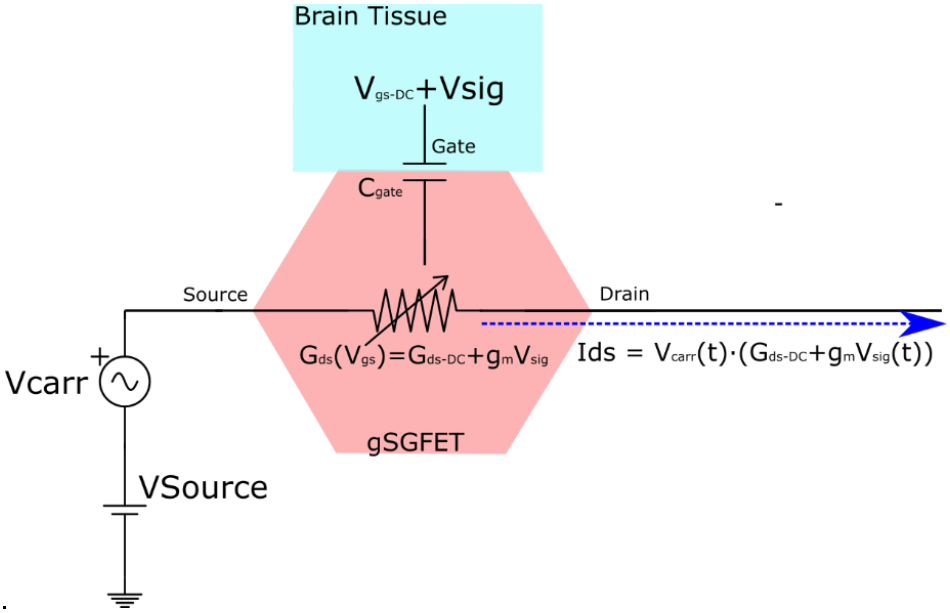

Figure 16 Basic scheme of gSGFET mixer functionality. The gate of the transistor, in contact with the brain tissue, is influenced by electrical potential fluctuations (neural signals) producing variations in the channel resistance and, as a consequence, in the current that flows through the transistor (I_{ds}). Then, I_{ds} is $V_{carr}(t)x(G_{ds\text{-}DC}+g_mV_{sig}(t))$ which is an AM modulation where $G_{ds\text{-}DC} = 1/R_{ds}$ and g_m is the transconductance of the transistor

The multiplication of those signals produces the folding of their frequencies, as can be seen in figure 17-left, where a peak at the carrier frequency (f_{c1}) is observed, with an amplitude proportional to channel resistant $R_{ds\text{-}DC}$, with two side bands at f_{c1}-f_{sig1} and f_{c1}+f_{sig} which are proportional to V_{sig}/g_m. The gate signal f_{sig1} is obtained after the demodulation process (figure 17-right).

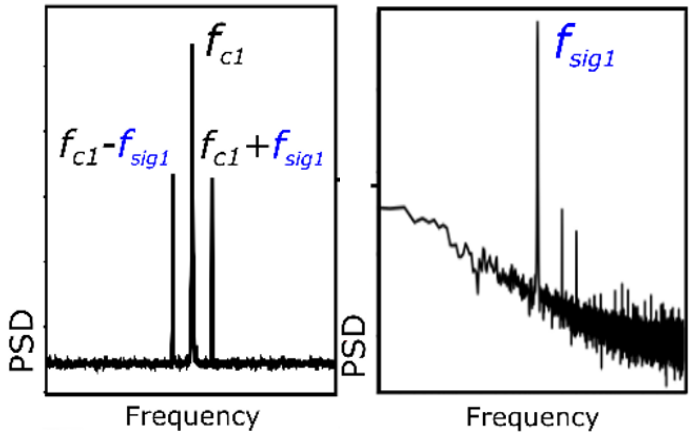

Figure 17 PSD of a modulated and demodulated signal. A pure tone carrier of frequency f_{c1} is modulated with a signal of frequency f_{sig1}. After the demodulation process f_{sig1} is recovered and the 1/f noise of the transistor can be observed. Figure adapted from [18]

3.1.3 Protection components

During a normal operation, the leakage current is controlled by the *gSGFET* gate impedance (figure 18a), being in the range of 1 nA (figure 18b) (3 orders of magnitude below the minimum of 10µA stablished by the regulation). However, in the case of simple failure (i.e. bias voltages exceeds the potential windows of *gSGFET* due to an electronics breakdown), the leakage current is not limited by any passive electronic component and could exceed the maximum allowed value of 50µA.

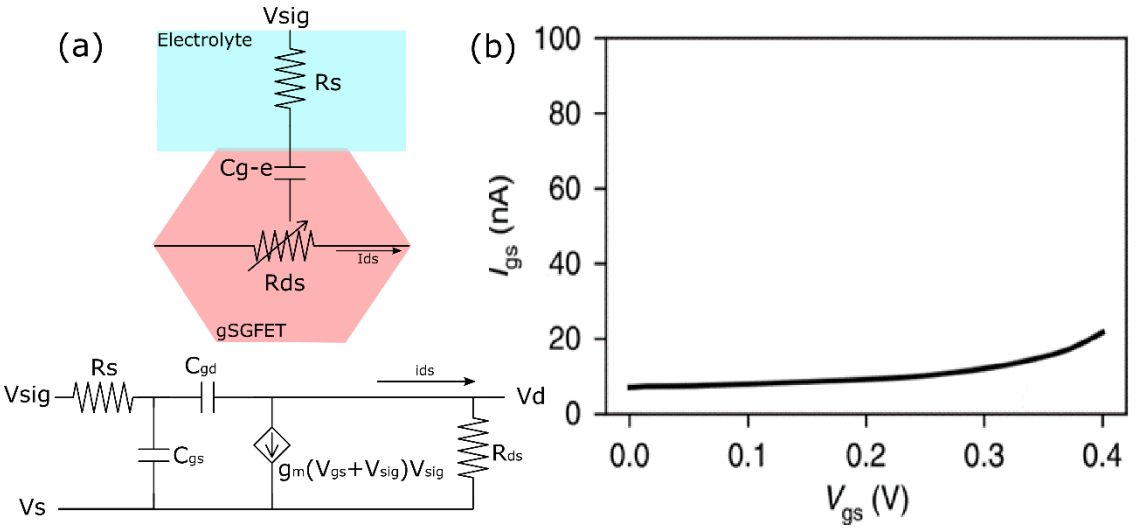

Figure 18 a) gSGFET structure where the channel is represented with a variable resistance and the gate impedance is defined by the gate capacitance $C_{g\text{-}e}$ (composed of C_{gs} and C_{gd}). b) Leakage current through $C_{g\text{-}e}$ during normal operation mode . Lower than 10µA (IEC60601-1). Figure adapted from [19]

To control the bias point of the transistor it is needed to control the DC voltage between the gate and the source. For that, the resistance R_{DC} is placed in parallel to *Cs*, which is connected to a DC voltage source. Figure 19 shows the gSGFET equivalent circuit connected to the signal acquisition system together with the protective elements (*Cs*, *Cd*, R_{DC}). It can be observed how the $I_{leakage}$ is ~0 in a stationary regime, when the gate capacitance ($C_{g\text{-}e}$) and protective capacitances (*Cd*, *Cs*) are charged at the source voltage (V_{source}).

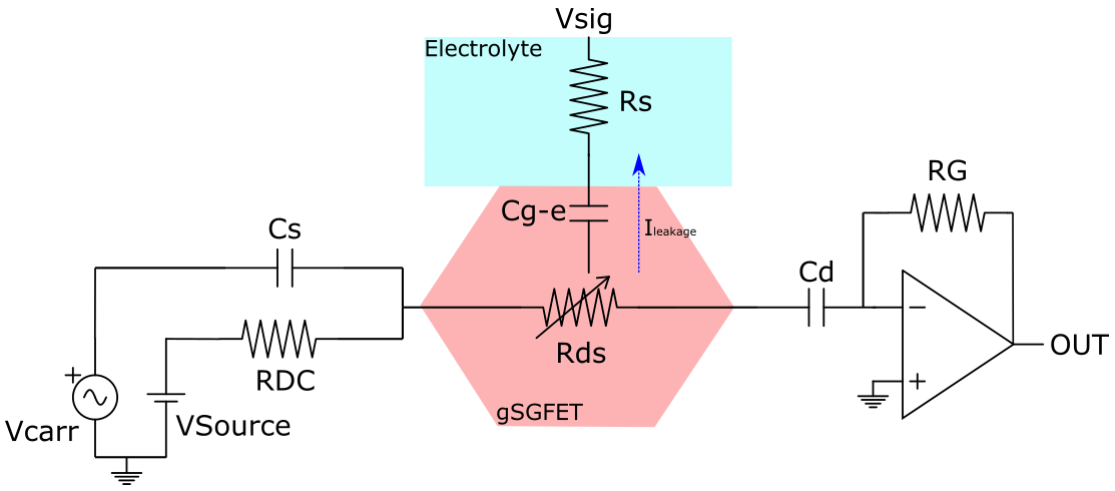

Figure 19 gSGFET equivalent circuit connected to *AC coupled system. Cd and Cs avoid DC current to pass through the transistor while R_{DC} is used to achieve the optimal bias point. When $C_{g\text{-}e}$, Cd and Cs are completely charged the system is stable, the leakage current through $C_{g\text{-}e}$ is very low and Vsig can be correctly recorded.*

If any electronics or device failure occurs the maximum allowed leakage current will be limited by the resistance R_{DC}. To accomplish with the regulation, the R_{DC} value should be high enough to limit the current through itself to a maximum value of 50µA. For that, the worst case scenario is chosen, which is when any of the circuit nodes have the electronics supply voltage (V_{supply}). Thus, the value of R_{DC} have to be calculated as:

$$R_{DC} > \frac{V_{supply}}{50\mu A} \tag{8}$$

To achieve a correct functionality of the AC coupling system, the value of the capacitors Cd and Cs should be chosen according with the frequency of the carrier signal (f_c) to avoid signal attenuation produced by the frequency response of the filters created by introducing these passive elements.

For C_S capacitance value it has to be considered the RC high pass filter (figure 20) composed by C_S in parallel with R_{DC} and R_{ds} (transistor's channel resistance). Accordingly the C_S value has to accomplish the following expression:

$$f_c > \frac{1}{C_s \cdot (R_{ds} // R_{DC})} \tag{9}$$

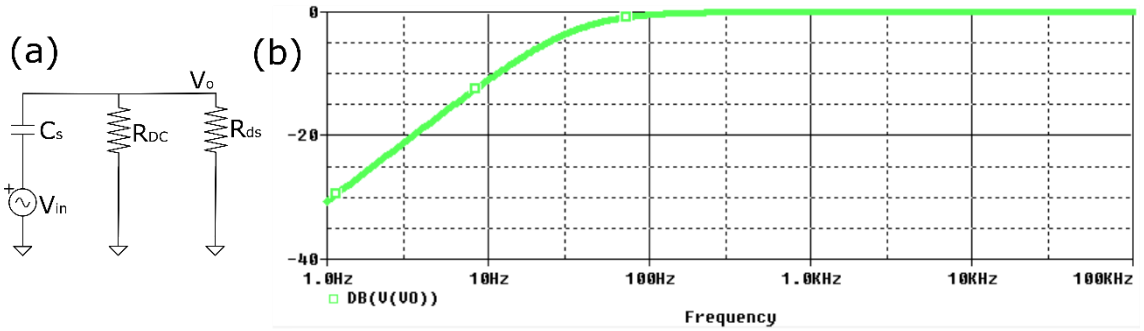

Figure 20 a) Passive high pass filter conformed by C_S in parallel with R_{DC} and R_{ds}, where R_{ds} is the transistor's channel resistance and C_S and R_{DC} are the elements added to accomplish IEC60601-1. b) Example of a frequency response obtained with Capture Pspice after execute the simulation of the passive high pass filter. The values used in the simulation has been: C_S = 4.7µF; R_{DC} = 100kΩ; R_{ds} = 1kΩ

For C_d capacitance calculation, the active high pass filter of figure 21 composed by C_d, the transistor's channel resistance, R_{ds}, and the resistance provided by the I-V converter at acquisition electronics (R_G), must be considered. The transfer function obtained from this filter is:

$$H(s) = \frac{V_o}{V_{in}} = -\frac{R_G}{R_{ds}} \cdot \frac{s}{1 + s \cdot (C_d \cdot R_{ds})} \tag{10}$$

As it can be seen the filter has a negative gain (inverted 180º) of value:

$$G = -\frac{R_G}{R_{ds}} \tag{11}$$

And it exists a pole at f_c which means that C_d has to accomplish the expression:

$$f_c > \frac{1}{2 \cdot \pi \cdot C_d \cdot R_{ds}} \tag{12}$$

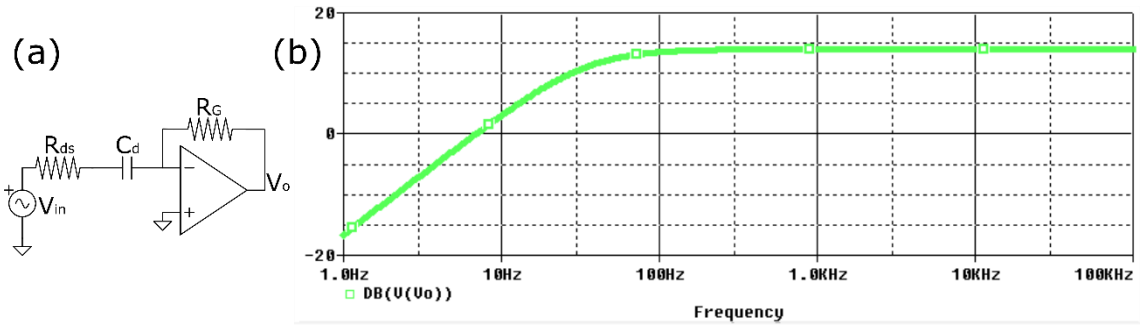

Figure 21a) Passive high pass filter conformed by C_d, R_{DC} and R_{ds}, where R_{ds} is the transistor's channel resistance, C_S is an element added to accomplish IEC60601-1 and R_G is the feedback resistance. b) Example of a frequency response obtained with Capture Pspice after execute the simulation of the passive high pass filter. The values used in the simulation has been: C_S = 4.7µF; R_G = 5kΩ; R_{ds} = 1kΩ

When choosing capacitances values it has to be considered that transistor's channel resistance value may vary from device to device, being standard values for gSGFETs between 1kΩ and 2kΩ. To ensure that f_c is not under the cut-off frequency of the filters worst case for R_{ds} must be considered.

3.1.4 Non-Idealities of protection components

Passive elements experience different effects due to the electric current going through them. It is important to pay attention and consider these effects as they can affect the electronic acquisition system and the recorded signals.

Figure 22 Representation of the Thermal Noise introduced by a resistor. A voltage source e_{nT} is connected in series with the resistor (R_{DC}) to represent the noise produced by the thermic excitation of electrons inside the conductor.

Thermal noise is represented as a voltage source in series with the resistor (figure 22) and is calculated accordingly with expression 13, where 'k' is Boltzmann's constant and temperature is fixed at 25ºC in Kelvin units:

$$e_{nT}^2 = 4 \cdot k \cdot T(K) \cdot R_{DC} \tag{13}$$

$$k = 1.38064852 \cdot 10^{-23}\, J/K$$

$$T(K) = 25ºC + 273.15 = 298.15K$$

$$e_{nT}^2 = 4 \cdot 1.38064852 \cdot 10^{-23} \cdot 298.15 \cdot 100 \cdot 10^3$$

$$e_{nT}^2 = 1.6465 \cdot 10^{-15} V^2$$

$$e_{nT} = 40.5778\, nV$$

Thermal noise introduced by R_{DC} is coupled to the carrier signal as current noise. Thus, interfering in the AM modulation of the drain-to-source current of gSGFETs. The calculated value has to be divided by channel resistance to obtain equivalent current noise. Therefore thermal noise value is lower enough to not affect to recorded signals.

Resistance R_{DC} also affects to the stabilisation time of the system because of its influence on capacitors charging time. When the system starts, capacitors are not charged, and the current (I) through each one sharply increases to its maximum value (I_{max}):

$$I_{max} = \frac{V_{Source}}{R_{DC}} \tag{14}$$

Progressively this current decreases as the charge of the capacitors grows up (figure 23) until capacitor's voltage (V_C) achieves 63.2% of the voltage source. At this moment capacitors are charged enough to consider that the acquisition system is stable, the time elapsed between turn on the system and this point is known as time constant and it is calculated with the following expression:

$$\tau_C = C \cdot R_{DC} \tag{15}$$

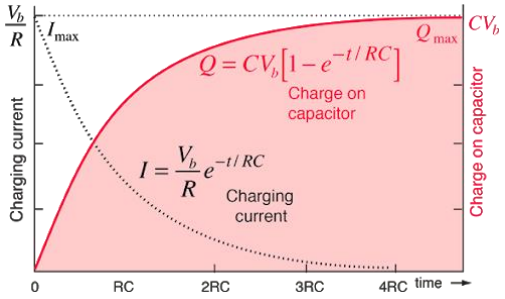

Figure 23 Charging process of a capacitor. Black pointed line indicates the current I_C that achieves its maximum value when the capacitor is totally discharged and decreases progressively until its value is close to 0A. Red line indicates the capacitor charging process from 0 to Q_{max}. Figure adapted from [20]

Time constant of capacitors is important when doing characterization of devices, especially to obtain the real transfer curve of the transistors, which gives information about the optimal bias point in which to polarize each transistor to improve their behaviour.

The transfer curve of a transistor is done obtaining the current I_{ds} for different values of V_{Source}. This means that for each sweep the acquisition system must wait to save data until all capacitors are completely charged and the system has achieved a steady state, which usually occurs at $5\tau_C$, depending on the initial state of the capacitors. To ensure the compliance of this condition, the acquisition system must wait a specified time for each V_{Source} change or, to optimize the time needed for the system calibration, use a stability detector to notice when the steady-state has been reached to start saving characterization data.

3.2 gSGFET frequency response

Transistor's non-idealities affects the AC coupled system by introducing harmonic distortion to the recorded signal read from the gate (V_{sig}) and to the carrier signals (V_{carr}). Harmonic distortion must be taken into account when choosing carrier frequency to ensure a proper AM modulation and demodulation.

3.2.1 Gate-Source signal distortion

The electrochemical potential in the electrolyte (V_{gs}) couples with the channel through the graphene-electrolyte interface capacitance (C_{gate}) producing a change in the number of charge carriers in the graphene channel and a variation in the drain-source current (I_{ds-sig}) for a constant drain-source voltage (V_{ds}). The current changes are proportional to the gate signal (V_{gs-sig}) and to the transconductance (G_m) which represents the transfer function of the device (figure 24a). Non-linearities in the transfer curve lead to a dependence with V_{gs} and to harmonic distortion of the signal (figure 24b).

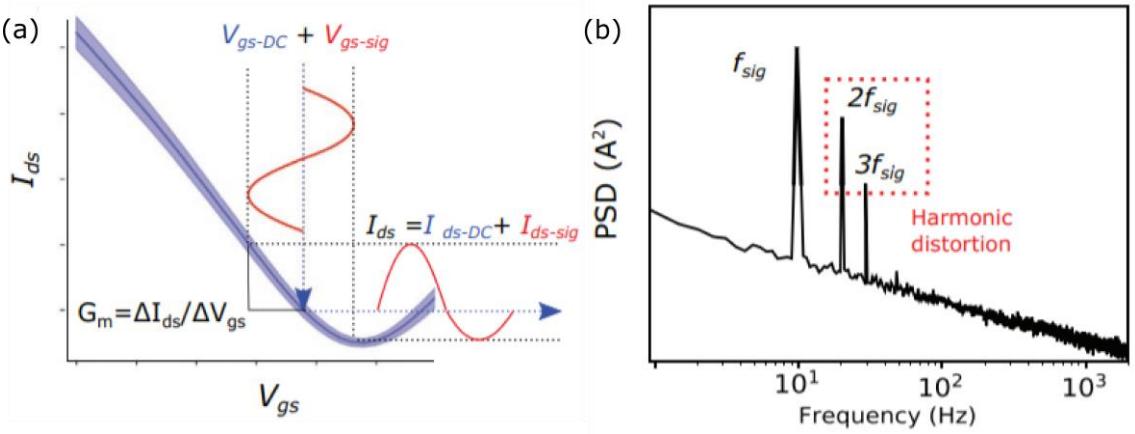

Figure 24 Figures adapted from [21] a) Standard transfer curve of a gSGFET (I_{ds} vs V_{gs}). G_m is indicated as $\Delta I_{ds}/\Delta V_{gs}$. V_{gs-DC} indicates the DC polarization of the active transducer while V_{gs-sig} represents the signal applied on the gate of the device. b) Standard PSD of a distorted output signal of a gSGFET. Harmonic distortion on the 10Hz (f_{sig}) results in the appearance of harmonic components at $f=2f_{sig}$ and $3f_{sig}$.

Ideally GSFETs present a linear I_{ds}-V_{gs} relation far from the conduction minimum (charge neutrality point) [22]. However, the conductance of the transistor is limited by the resistance between the metal contacts and the graphene channel resulting in a curved I_{ds}-V_{gs} relation away from the CNP. The conductance minimum at the CNP should be perfectly sharp but the inhomogeneous doping of the graphene channel due to substrate inhomogeneities lead to a broadening of the CNP.

gSGFETs response non-linearities impede to obtain V_{sig} pure tone at I_{ds} producing flattening or loose of symmetry which leads on harmonic distortion which can be calculated using the Taylor expansion of the stationary I_{ds}-V_{gs} curves. The expansion to the 3rd order can be express using the following expression:

$$I_{ds} = I_{ds|V_{gs}0} + \left.\frac{dI_{ds}}{dV_{gs}}\right|_{V_{gs}0} A_{sig}\sin(2\pi f t) + \frac{1}{2!}\left.\frac{d^2 I_{ds}}{dV_{gs}{}^2}\right|_{V_{gs}0} \frac{A_{sig}{}^2}{2}\sin(4\pi f t) + \frac{1}{3!}\left.\frac{d^3 I_{ds}}{dV_{gs}{}^3}\right|_{V_{gs}0} \frac{A_{sig}{}^3}{4}\sin(6\pi f t) \qquad (16)$$

Experimentally, harmonic distortion introduced by gSGFETs, usually is characterized applying a pure tone test signal ($V_{gs\text{-}sig}$), that ideally should not have distortion, and measuring the higher order harmonics generated by the signal distortion (1st, 2nd and 3rd harmonics).

To validate the stationary description of harmonic distortion a comparison has to be done between the calculated expression and the measured signals when applying an $8mV_{rms}$ in a wide range of V_{gs} for a 10Hz frequency [21]. Figure 25a shows very good agreement for 1st, 2nd and 3rd harmonic, being this last one close to gSGFETs noise that, for small values of A_{sig}, masks the low amplitude of 3rd harmonic (figure 25b).

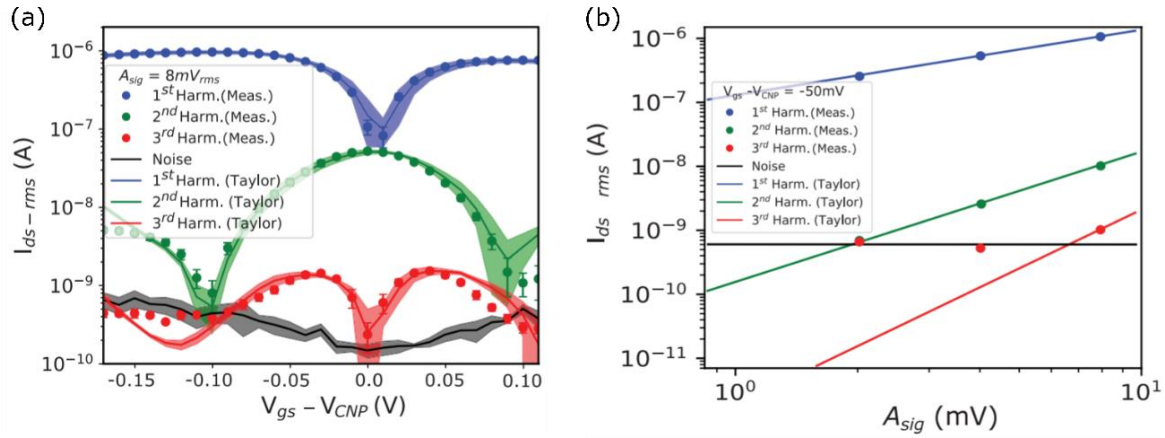

Figure 25 Figures adapted from [21] a) 1st, 2nd and 3rd harmonics rms-amplitude extracted from the power spectrum of the measured I_{ds} for a signal with A_{sig} = 8mV_{rms} and f_{sig}=10Hz (dots) and from the taylor expansion of the transfer characteristics (solid lines). Noise evaluated from the power spectrum at 28Hz is also represented (black line) b) Harmonics obtained for different signal amplitudes (2, 4 and 8 mV_{rms}) are represented (dots) also with the calculated values derived from Taylor expansion. The data was evaluated at V_{gs}-V_{CNP}=-0.05V.

The signal-to-distortion ratio (SDR) is a figure of merit used to evaluate distortion impact on the signal quality for any combination of A_{sig} and V_{gs} (figure 26a). SDR presents a

maximum at V_{gs}-V_{CNP} ≈ 100mV indicating the point where I_{ds}-V_{gs} curve linearity is maximum. Close to CNP there is a minimum produced by the drop of trasnconductance and the increase of the 2nd order harmonic amplitude. The linear, quadratic and cubic relation between the three harmonics and A_{sig} explains the increase of SDR when A_{sig} is reduced.

Comparing the harmonic distortion with the intrinsic 1/f gSGFETs noise DNR (distortion-to-noise ratio) can be obtained (figure 26b). It shows its maximum at CNP, its minimum at V_{gs}-V_{CNP} ≈ 100mVm and decreases with A_{sig} value. The parameters for which distortion and noise contribute with the same power to the signal quality degradation are indicated by the 0dB contour line.

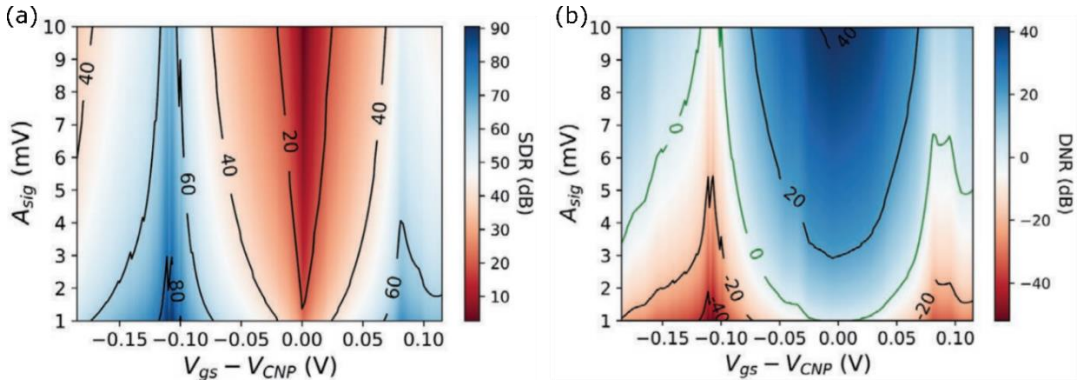

Figure 26 SDR evaluation (a) and DNR evaluation (b) in DB in the A_{sig}-V_{gs} parameter map. Solid lines indicate the contour lines every 20dBs. Maps are calculated using the Taylor expansion of stationary I_{ds}-V_{gs} curves. Figures adapted from [21]

3.2.2 Carrier signal distortion

In DC operation the drain-to-source voltage bias produces a change in the Fermi level of the graphene with respect to the vacuum level. When brought in contact with the electrolyte gate, graphene and electrolyte Fermi energy equalises producing a shift in the Dirac energy with respect the Fermi energy which cause an accumulation of charges at the graphene-electrolyte interface (figure 27a-mid) and a shift in the CNP for different V_{ds} values (figure 27b). The oscillatory drain-to-source voltage applied at the AM coupled system (figure 27a-top-bottom) avoid this shift in the CNP for different V_{ds} (figure 27c).

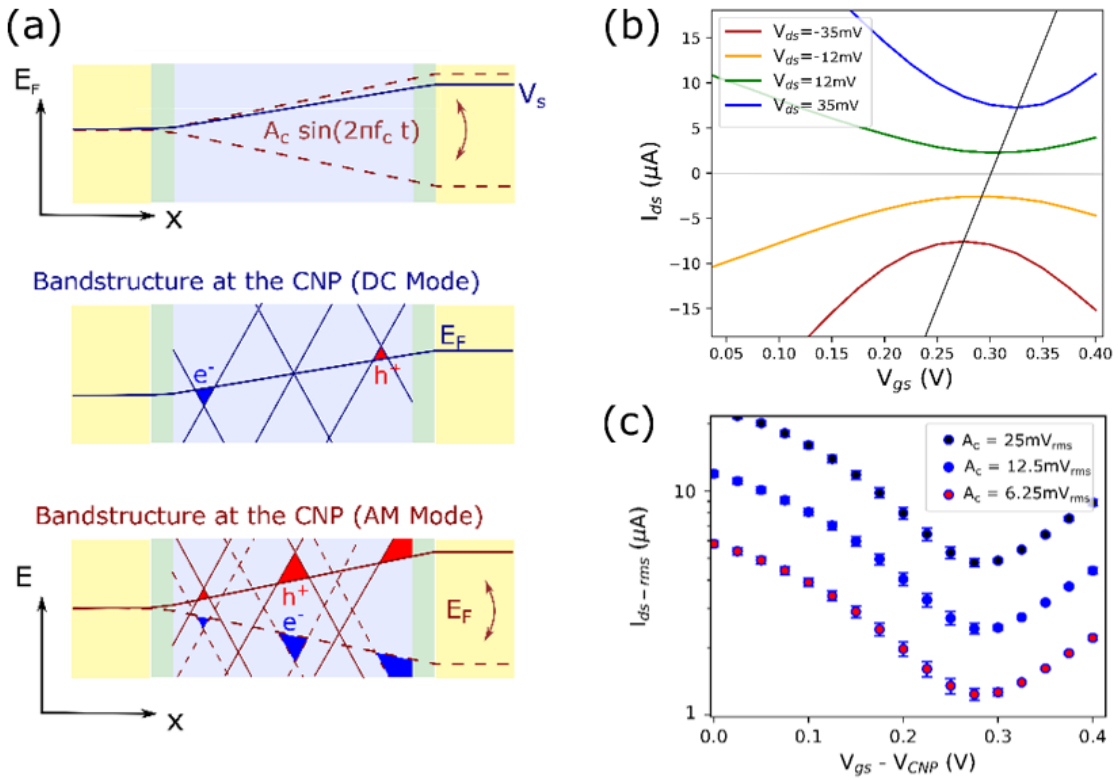

Figure 27 Figures adapted from [21] Supporting information a) Fermi energy in the graphene (top) for DC (solid) and AM (dashed) modes. Band structure at the CNP is shown along the graphene channel for the DC (mid) and AM (bottom) modes. b) I_{ds}-V_{gs} curves for different values of V_{ds} in DC mode. Black line indicates the CNP shift. c) I_{ds}-V_{gs} curves for different carrier amplitudes in AM mode.

In AM mode, unlike DC mode (figure 28b-left), the gSGFET is not operating at a stationary point in the V_{gs}-V_{ds} plane (figure 28a) due to the oscillation of the drain-source bias along the V_{ds} axis. In this way, I_{ds}-V_{ds} curves (figure 28b-right) non-linearities lead to a distortion of the carrier signal producing harmonics at frequencies multiple of f_c (figure 28c).

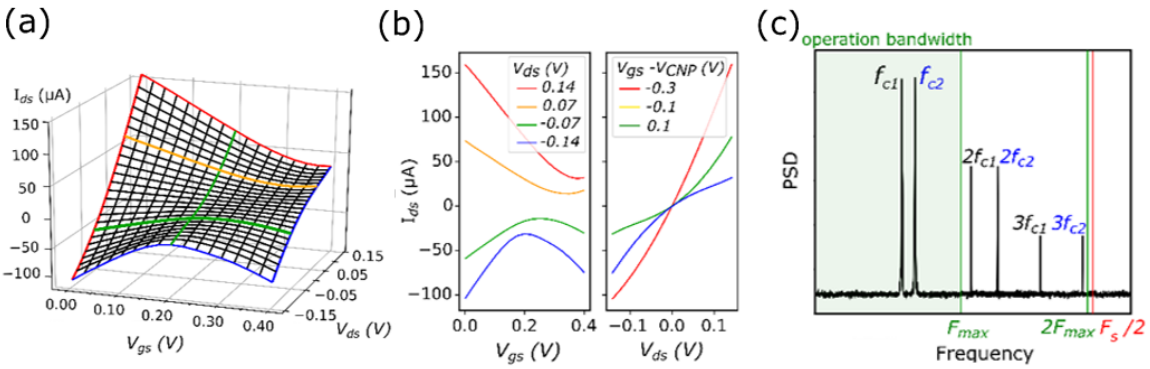

Figure 28 Figures adapted from [18] a) 3D representation of I_{ds} dependence on V_{gs} and V_{ds}. b) I_{ds}-V_{gs} CNP shift (left) and I_{ds}-V_{ds} non-linearities (right) produced by the effective gating. c) Two carrier signals with their 2nd and 3rd harmonics. Operation Bandwith is marked with green zone and Nyquist frequency (F_s/2) with red line.

When choosing carrier frequencies, high order harmonics must be taken into account to avoid them to lie within the frequency bandwidth dedicated to acquired signals. This means, if you are about to record signals below 1kHz frequency, the operation bandwidth (figure 28c), which goes from f_c-1kHz to f_c+1kHz, must be free of harmonics.

3.2.3 Channel impedance

gSGFET can be illustrated as the contact resistance (R_c) in series with a set of resistive elements that represents the graphene sheet resistance (R_{ds}). At low frequencies the capacitive elements that represents the graphene-electrolyte interface ($C_{g\text{-}e}$) show a significantly larger impedance ($Z_c = \frac{1}{2\pi f C}$) than the channel resistance of the transistor (figure 29-top). As frequency increases, interfacial capacitive elements impedance decreases, leading on a leakage of part of the drain-to-source injected signal through the graphene-electrolyte interface due to the appearance of an alternative conduction path through $C_{g\text{-}e}$ and the electrolyte (figure 29-mid). For high frequencies (figure 29-bottom) charge flows from drain to source mainly across the electrolyte instead of going along the graphene sheet. As a consequence, the frequency response of the transistor is dominated by the series resistance R_c.

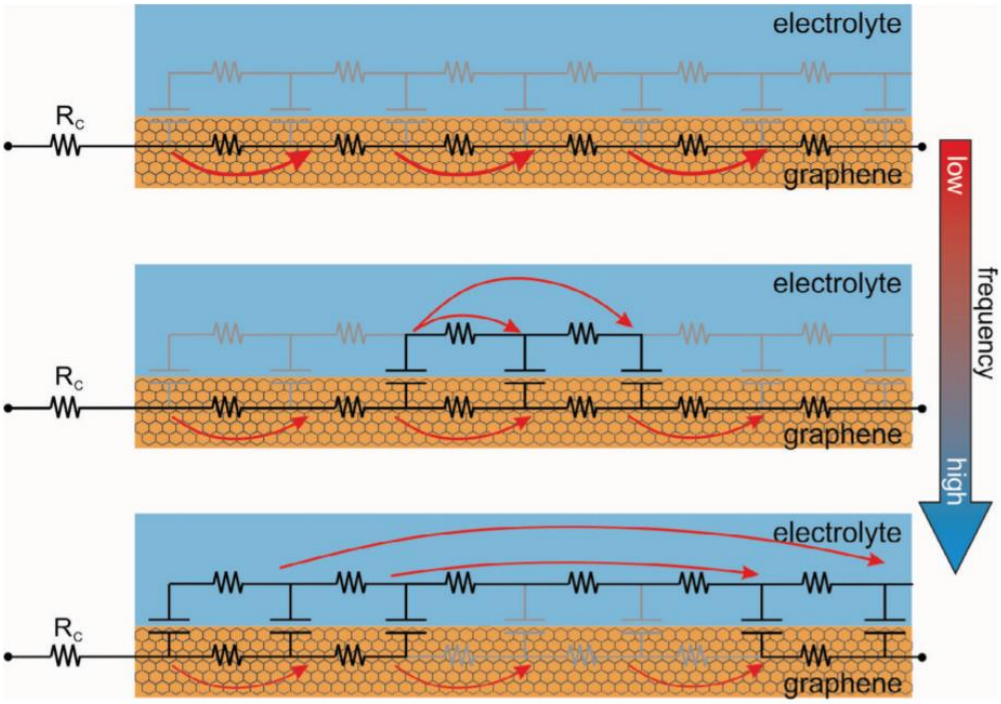

Figure 29 Illustration of the circuit elements that contribute to the current density at the graphene-electrolyte interface from low (top) to high (bottom) frequencies. Figure adapted from [23]

The cut-off frequency of this phenomenon appears at higher frequencies for shorter channel lengths thanks to the high ratio between mobility and interface capacitance in graphene. The frequency response of gSGFET for different channel lengths is shown in figure 30 proving an approximately constant response at carrier frequencies lower than 500 kHz for channels with a maximum length of 100µm.

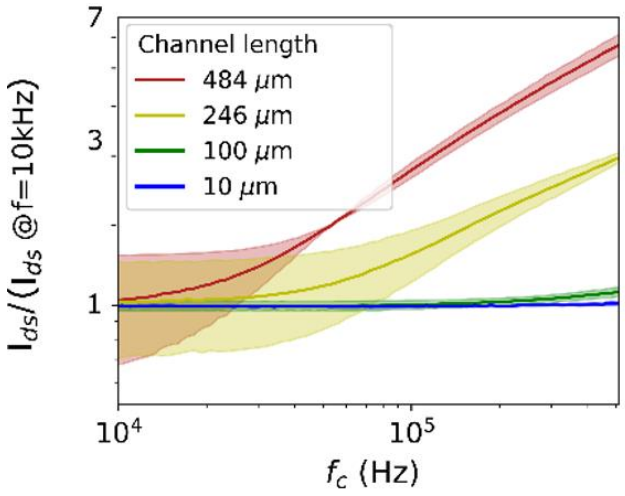

Figure 30 I_{ds} normalized by its value at 10 kHz for different channel lengths and its standard deviation (filled area). Figure adapted from [18]

3.2.4 Carrier and Sampling Frequency considerations

In order to achieve a correct recording of gate signals (V_{sig}) it is important to choose appropriate values of carrier frequencies taking into account the frequency response of gSGFETs but also, the harmonic distortion produced by non-idealities of the devices.

Also, acquisition sampling frequency influences on harmonics folding. It is limited by the acquisition card used. Sampling frequency of the acquisition card used in this system is limited depending on the acquisition channels used as shown in table 1.

Taking into account the acquisition card is capable of reading a maximum of 16 channels (in differential mode), the maximum sampling frequency permitted to be used in the system is calculated at expression 17.

Table 1

Number of Channels	Sample rate
1	2.00 MSample/s
2	1.00 MSample/s
≥ 3	$\frac{2.00\ \text{MSample/s}}{nChannels}$

$$f_{s\_max} = \frac{2\ MHz}{16\ Chn} = 125\ kHz \tag{17}$$

Nyquist theorem defines the maximum carrier frequency that can be used, for a specific sampling frequency, to avoid aliasing. As commented in a previous chapter, carrier signal is distorted producing harmonics at multiple values of its frequency. For this reason, carrier frequency must be chosen to avoid 2nd order harmonic folding into the band of operation.

$$f_{carr\_max} \leq \frac{f_{s\_max}}{2 \cdot 2} = \frac{125\ kHz}{4} = 31.250\ kHz \tag{18}$$

Taking into account all the requirements about the gSGFETs frequency response and harmonic distortion, and considering a transistor array of 1 column and 16 rows, with a maximum channel length of 240µm, and an acquisition system which maximum sampling frequency is 125 kHz, valid carrier frequency values for the pure tone applied as drain-to-source signal should be f_{carr} = 20 kHz and f_{carr} = 30 kHz. Notice that, although 20kHz carrier avoid $3f_c$ harmonic folding, both frequencies provide the same operational bandwidth of 5kHz (figure 31).

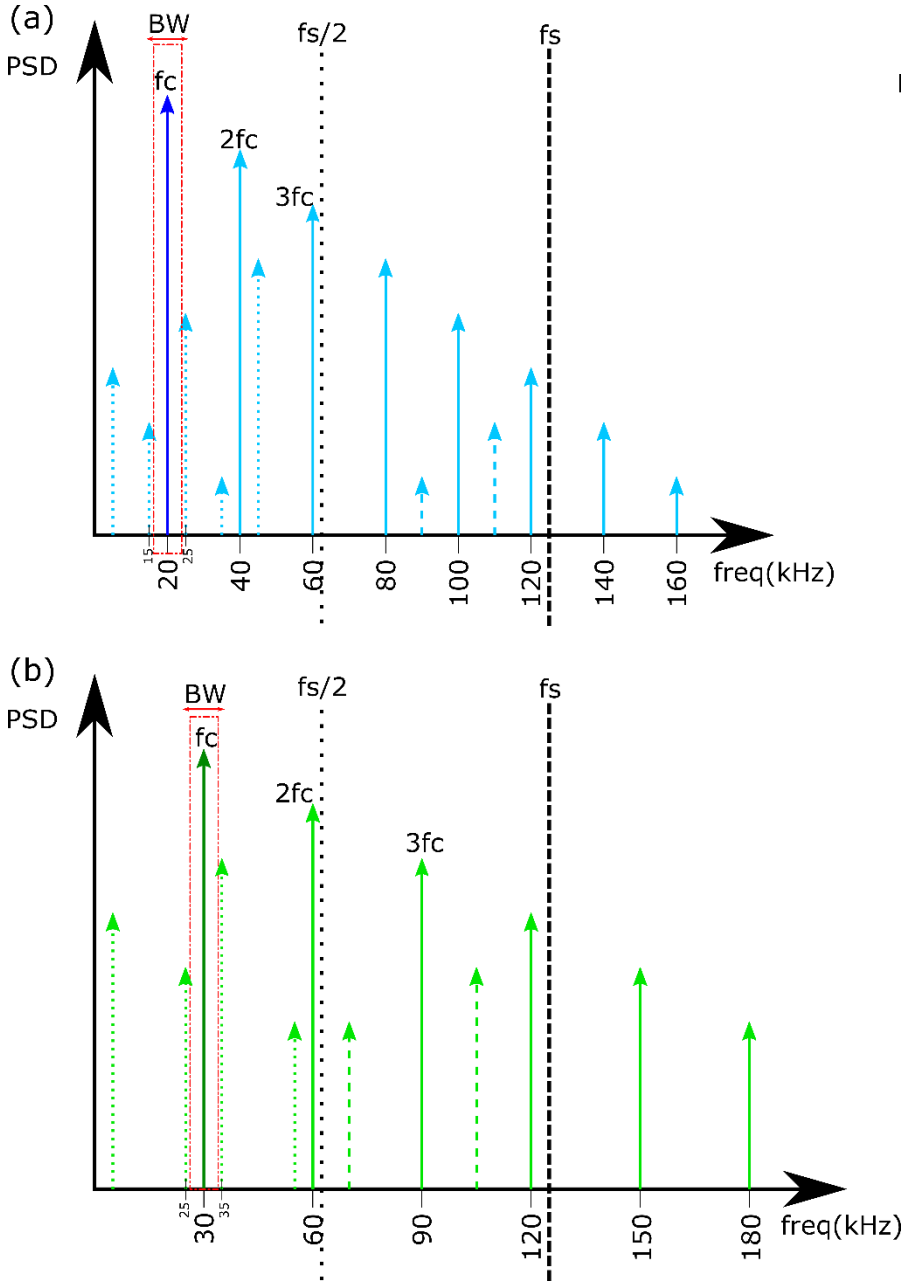

Figure 31 Harmonic study for 20kHz (a) and 30kHz (b) carrier frequencies. Fs/2 and Fs frequencies that produce folding and mirroring of harmonics into carrier band are indicated with pointed and dashed vertical lines. Operational bandwidth, zone where an AM modulation can be successful avoiding harmonic interferences, is limited by a red square.

4 Acquisition System

The block diagram of figure 32 illustrate the acquisition system implemented to achieve signal recording using gSGFETs. The system is divided in two parts, generation module and acquisition module. The first one is used to condition carrier signal (V_{carr}) and polarization voltage (V_{DC}) introduced as source voltage of the transistor (V_{Source}). The second one is responsible of adapting the recorded signal (V_{Drain}) to be read by the ADC. Also a software processing stage is necessary to process the recorded signal and obtain the original signal introduced in the gate of the devices (V_{Gate}).

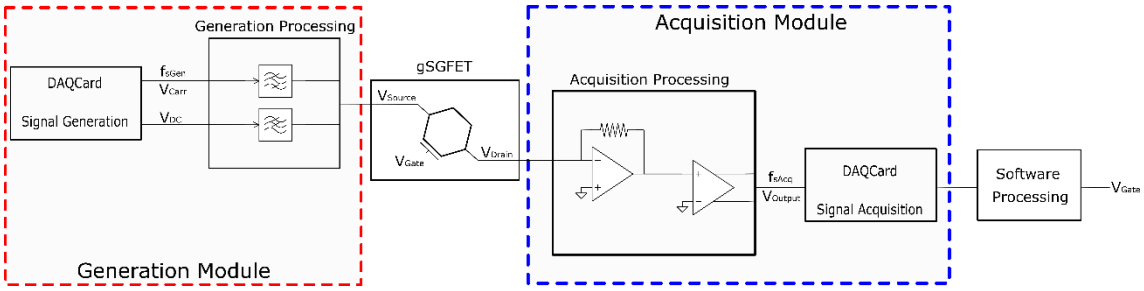

Figure 32 Block diagram of the acquisition system implemented to achieve gSGFET signal recording. The gSGFET is polarized with the voltage (V_{Source}) obtained from the generation module (red squared). V_{Drain} is processed with the acquisition module (blue squared) achieving, after a software processing, V_{Gate}.

4.1 Acquisition Card

The acquisition card is used for the generation of carrier signals and DC voltages needed to polarize the transistor (V_{carr} and V_{DC}) and also, as interface between the electronic acquisition module and the computer. Its configuration is done using a software program that permits to modify main parameters used for the recording of signals in accordance with user requirements and computer limits.

The acquisition card chosen for this system has been DAQ Multifunction I/O Device USB 6363 (figure 33). Its specifications (Table 2) allows a maximum of 4 outputs and 16 inputs which permits the use of 1x16 arrays. Also its DAC number of bits and the possibility of modifying full scale voltage range give a way to improve the resolution of the system.

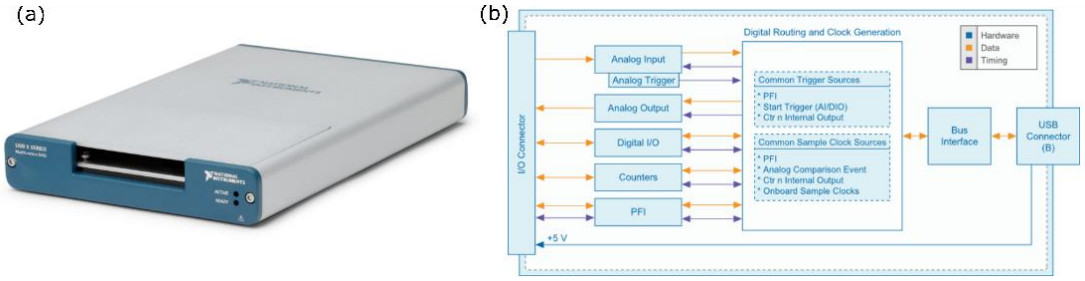

Figure 33 a) DAQCard USB-6363 Screw Terminal Pinout. b) Simplified block diagram of the USB-6363

Table 2

Specifications	Value
Analog Input Channels	32 single ended / 16 differential
Input Max Sampling Rate	2MS single channel / $\frac{2MS}{nChn}$ multichannel
Input Range	0.1; 0.2; 0.5; 1; 2; 5; 10 V
Maximum Input Voltage	11 V
Analog Output Channels	4
DAC Resolution	16 bits
Digital Input/Output channels	48

4.2 Electronic Circuit

The acquisition system requires of a generation module responsible of carrier and bias generation, and an acquisition module that mainly consists of an I-V converter. It is also needed a voltage supply module to power the operational amplifiers (V_{cc} and V_{dd}).

4.2.1 Voltage Supply

The voltage supply circuit of the system is powered by batteries to avoid 50Hz noise induced by the network. The circuit basically consist on a Boost converter (figure 34a) that increases input voltage from +4.2V to +5.5V and an inverting charge pump to achieve -5.5V (figure 34b). In order to achieve a more stable and noiseless signal, LDO regulators are implemented to obtain ±5V used as V_{cc} and V_{dd} of the operational amplifiers used in the main circuit.

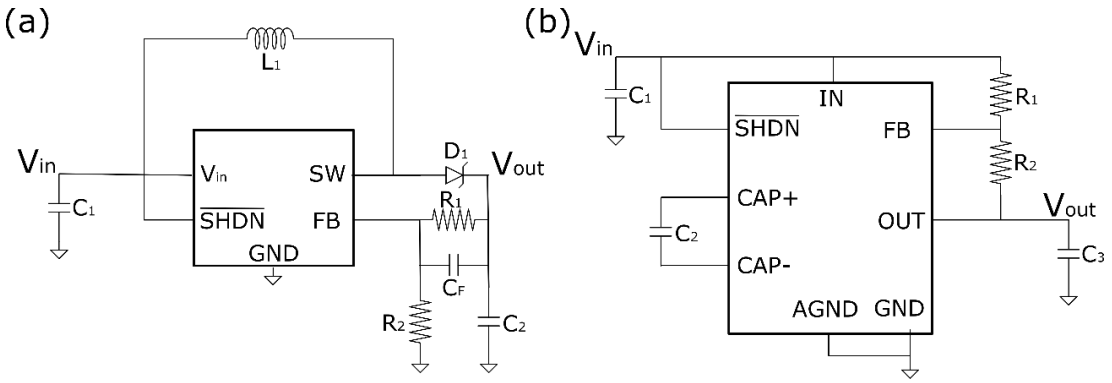

Figure 34 a) Boost converter typical application schematic obtained from LM2731 datasheet from Texas Instruments. b) Inverting charge pump typical operating circuit obtained from MAX889RESA datasheet from Maxim Integrated.

4.2.2 Carrier Generation

The DAQ card uses a digital to analog converter to generate the carrier signal used as drain-to-source voltage. As the generated signal must be a pure sinusoidal wave it has to be considered the sampling frequency value used (F_{sGen}). Due to the DAC, if F_{sGen} has a low value the signal generated is similar to a square waveform (figure 35), for this reason the maximum sampling frequency allowed by the acquisition card for the output channels has to be used (2MHz), ensuring that the signal generated is as close as possible to a sinusoidal waveform (figure 35). Also it has to be considered that carrier signal will always be generated with a finite sampling frequency which means it will introduce harmonics into the system [24].

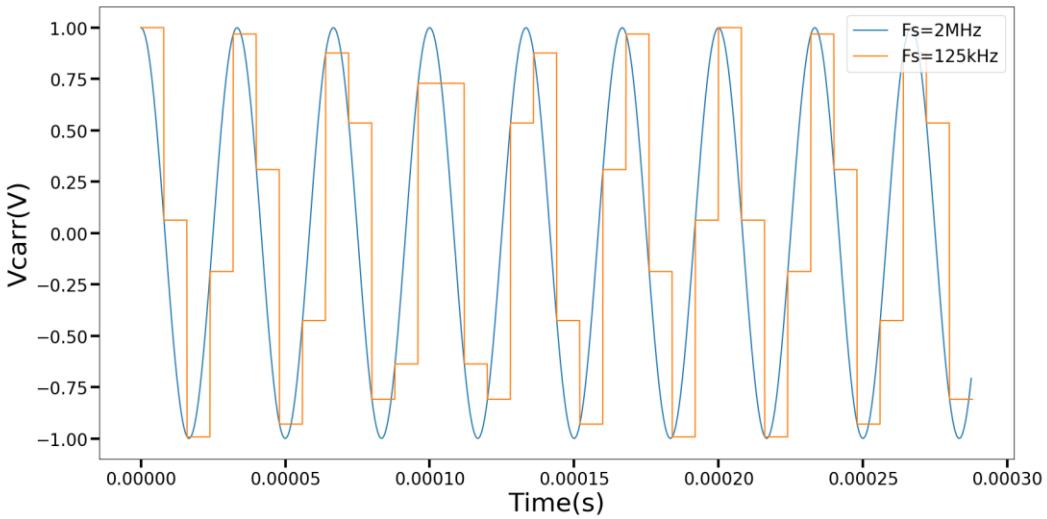

Figure 35 Simulation of the effect of sampling frequency on the digital to analogue converter when generating the carrier signal of Fc=30kHz. Blue line shows the DAC reconstructed signal with Fs=10MHz while orange line shows the reconstructed signal with Fs=120kHz

To avoid introducing these generated harmonics into the modulated signal through the carrier, a band pass filter has been designed. To achieve a narrow bandwidth a Dellyiannis-Friend Biquad has been implemented. This filter is useful thanks to the low sensibility of its parameters with the variation of passive components. Also its ENF structure (figure 36a) is usually used for middle and high frequency circuits because it reduces the effect of the operational amplifier frequency response on the filter behaviour (figure 36b).

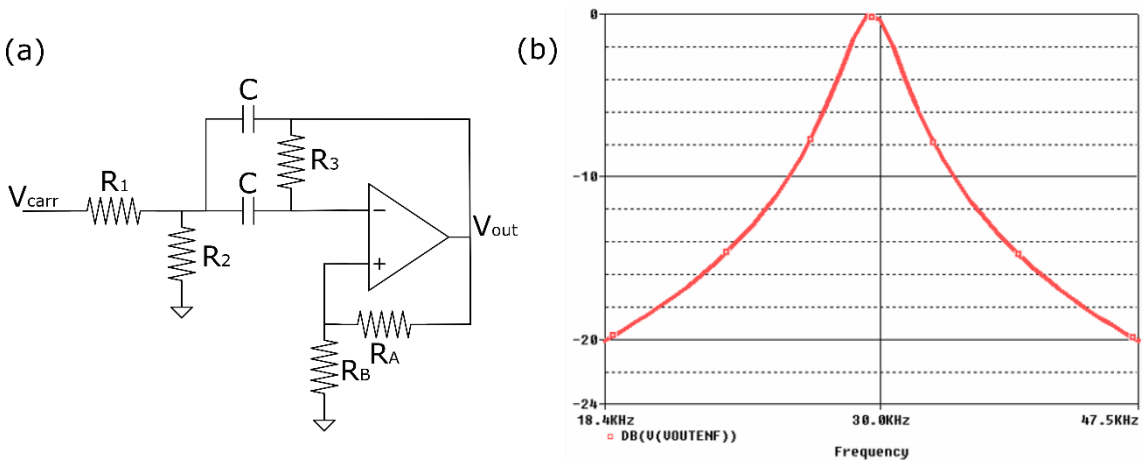

Figure 36 a) ENF structure of a Dellyanis-Friend Biquad which implements a band pass filter with gain, quality factor and bandwidth modifiable with passive components values. b) Simulated frequency response of the ENF structure with unitary gain using a real operational amplifier, a quality factor of 10, a central frequency at 30kHz and a bandwidth of 3kHz. A small shift of the central frequency is appreciated due to operational amplifier frequency response.

4.2.3 Bias Generation

The DC voltage used to polarize transistor's bias point is also generated with the DAQ Card as a common mode voltage for all the devices. This voltage needs to be as much flat as possible, ideally without any oscillation, for this reason a passive RC low pass filter (figure 37a) has been implemented between the DAQ Card output and the circuit input pin. Also, in order to decouple the signal generation from the main electronic circuit, a "follower" has been implemented (figure 37a) providing isolation of the circuit so that its power is not disturbed.

4.2.4 Current to Voltage converter

The treatment of the acquired signal is done using a current to voltage converter (figure 37b). The operational amplifier used needs to have a high slew rate, a low voltage noise and a low offset voltage to ensure the processed signal is not going to be affected by A.O intrinsic parameters. Also the capacitance in parallel with feedback resistor tries to compensate the decreasing open loop gain of the amplifier. The capacitance value has to be around Pico Farads order or lower to ensure a fast charge so that $I_{acq} = I_{RG}$ in order to not affect the output voltage of the circuit obtained, given as $V_{out} = \frac{I_{RG}}{R_G}$.

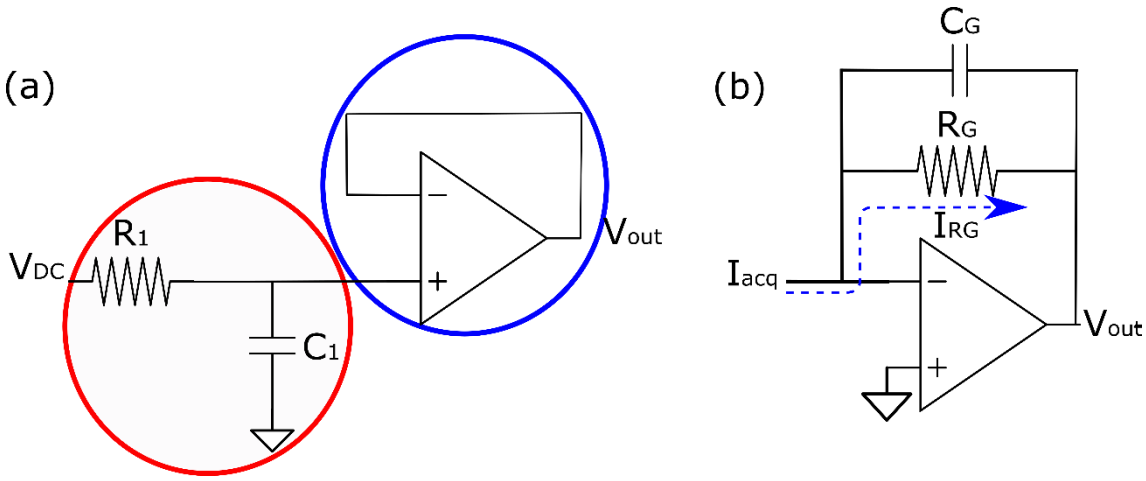

Figure 37 a) Electronic circuit implement to process the DC voltage generated by the DAQ Card. Red circle shows the low pass filter used to ensure the flatness of the bias voltage and blue circle shows the follower configuration used to isolate the main circuit from the power supply. b) Current to voltage converter use to obtain V_{out} from the acquired current (I_{aqc}).

4.3 Noise Design Considerations

The electronic system is employed for the acquisition of signals using gSGFETs as active transducers. In order to achieve a correct data recording is mandatory transistor's noise to be higher than electronic intrinsic noise, for this reason some noise design considerations has been taken into account adding some electronic to the main design.

4.3.1 Acquisition Noise

Operational amplifiers have an intrinsic low frequency noise, usually at frequencies below 1kHz, that is added into the output signal obtained. Although this noise will not affect the recovery of the recorded signals thanks to the high carrier frequency used for the AM modulation in the AC coupling system, it will increase the floor noise obtained from the entire system, making it difficult to achieve electronics noise to be lower than transistors ones. To avoid increased electronic floor noise due to operational amplifiers response, a high pass filter has been introduced after the current to voltage converter (figure 38) ensuring that the acquired signal is not affected by the amplifier intrinsic noise.

Also it has to be considered that operational amplifiers not only amplifies the desired signal but also the noise introduced at the input as common mode voltage. To reduce the effect of noise at the recorded signal a single to differential amplifier (figure 38) has been added at the I-V converter output. Additionally, a low pass filter has been applied to each differential output (figure 38) to attenuate high order harmonics produced due to gSGFETS and A.Os non-linearities.

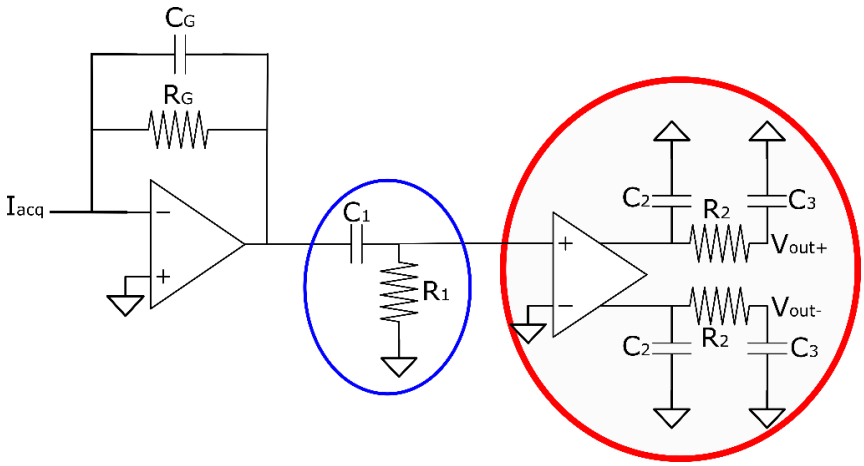

Figure 38 Current to voltage converter followed by a high pass filter (blue circle) and a single to differential converter whose outputs are connected to a low pass filter (red circle)

4.3.2 Power Supply Noise

To improve noise level and heat dissipation produced by the power flowing through the circuit, operational amplifiers supply voltages (V_{cc} and V_{dd}) have been distributed using plains in a specific "voltage" layer in the main board. Also ground plains have been created through two different layers (intermediate and bottom) being both interconnected with a huge number of via holes.

To avoid noise and distortions produced by operational amplifiers supply voltages (V_{cc} and V_{dd}) fluctuations, a capacitor set (figure 39) has been connected at the supply voltage pins of each operational amplifier used in the acquisition system, maintaining a DC supply voltage stabilized and without fluctuations as A.Os supply.

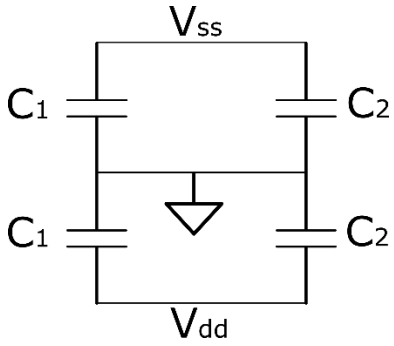

Figure 39 Capacitors Set to maintain stabilized operational amplifiers supply voltages.

4.4 Software

A software program, which can be found on GitHub [25], is needed to modify DAQ card main parameters of the acquisition system configuration. Python has been the programming language used for the software generation due to its open source character and the support given by National Instruments (DAQ card corporation) for acquisition card measurements and control units.

4.4.1 Graphical User Interface

A graphical user interface has been implemented to allow any user to configure and execute the recordings without the need of programming knowledge. To GUI generation it has been used the class "ParameterTree" from the external library named as "pyqtgraph" [26], which basically provides a way to handle hierarchies of parameters and upload changed parameters on the GUI automatically.

This software allows real time signal acquisition. The user needs to define the number of carriers to be used, frequency and amplitude of each one as well as bias common voltage used for transistor's polarization. Besides, acquisition main parameters are also needed such as sampling frequency, number of samples to acquire each cycle and the voltage range that determines the resolution of the recorded signal, and if demodulation is wanted to be done also in real time, down sampling factor.

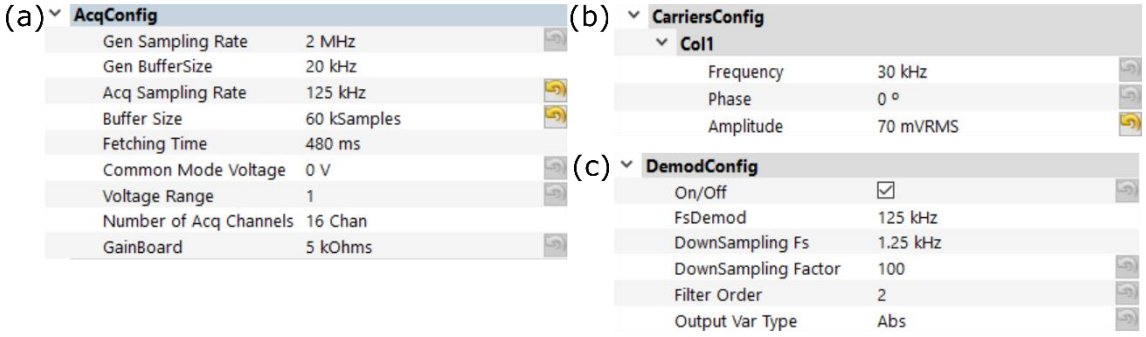

Figure 40 GUI parameters to configure real time acquisition. a) Configuration of the acquisition system which include Sampling Rates, number of samples acquired each fetch, bias voltage applied and dynamic range used. b) Carrier configuration where frequency and amplitude (RMS) applied to the carrier signal can be selected c) Configuration applied when demodulating in real time. The most important parameter is the down sampling factor. The type of output can be selected to show absolute, real, imaginary or angle output value.

On the other hand, if transistor's characterization is wanted to be performed, the user needs to introduce the gate-to-source voltage sweep as the initial and final values and the number of points to perform, and also, the drain-to-source voltage sweep. To ensure that the data is being saved after all the system is completely stable, which means all the capacitors are totally charged, a maximum slope allowed or a maximum waiting time can be defined.

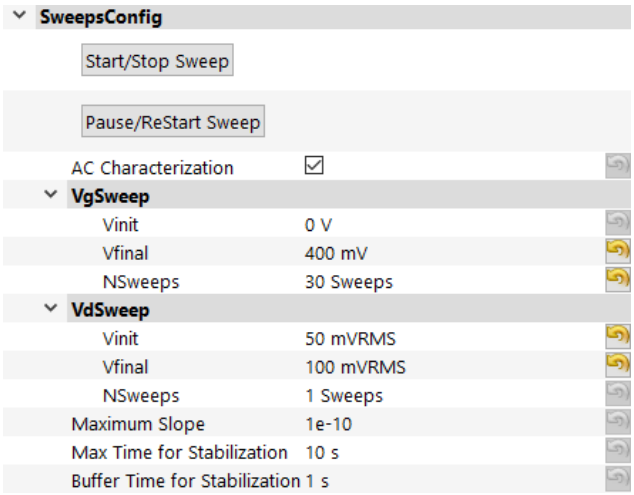

Figure 41 GUI parameters to configure characterization process. Bias voltage and carrier amplitude sweeps must be specified. Maximum slope and Time are used to ensure the stabilization of the system before saving data.

The characterization process provides a set of two dictionaries (DC and AC data) from which main transistor's parameters can be obtained such as transfer curve or transistor's noise. The transfer curve obtained is useful to determine the optimal bias point of each transistors array when performing a real time acquisition and also, to calibrate the recorded data to recover the desired signal (V_{sig}). Transistor noise indicates the minimum signal amplitude that the system will be able to recover, so if the noise is higher than the recorded signal the system will be unable to differentiate between signal and noise. For this reason transistor's noise is expected to be around 20µV, allowing the recording of signals up to 50µV.

4.4.2 Characterization Process

Characterization process (figure 42) consist in the measurement of transistors current for different values of bias voltage applying a specific carrier amplitude. As it is a real time measurement several processes are executed at the same time to avoid missing data. Acquisition, demodulation and stability detector processes are the main ones that need to be completely blended because they are daisy chained.

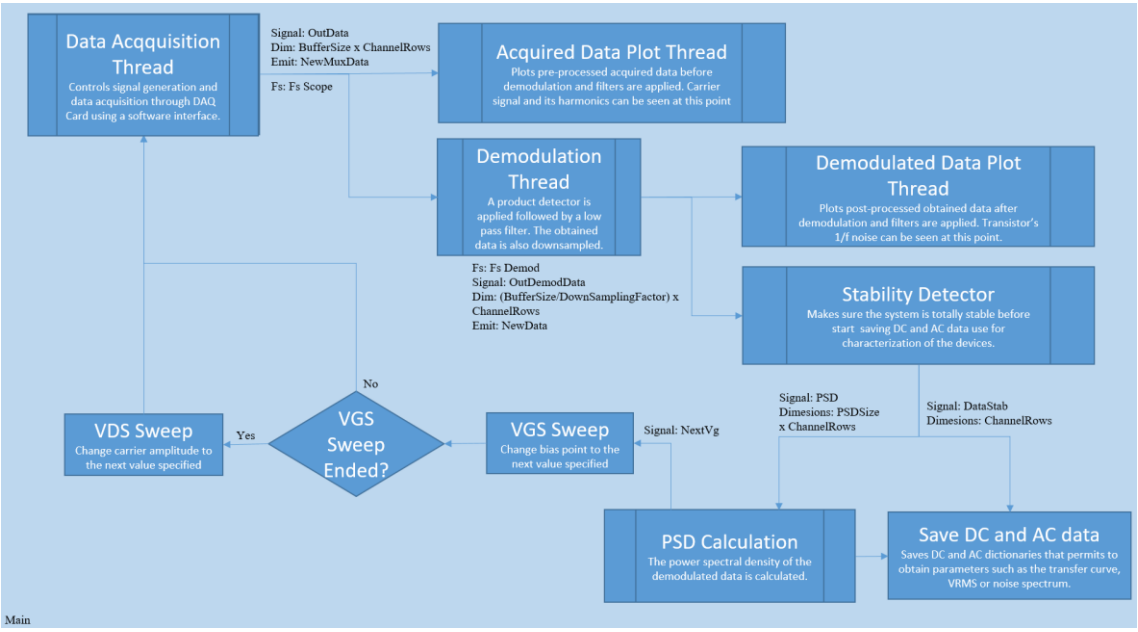

Figure 42 Flowchart of software used for real time gSGFET's characterization process. Signals and its dimensions of each process step are specifies as well as emitted signals or sampling frequency.

The acquisition thread (figure 43) is used for calculating carrier and local oscillator signal. This process starts DAQ card generation signal to polarize the transistors with V_{carr} and V_{DC} and also is responsible of starting and control data acquisition, notifying the system when it has been obtained enough data to execute the demodulation process.

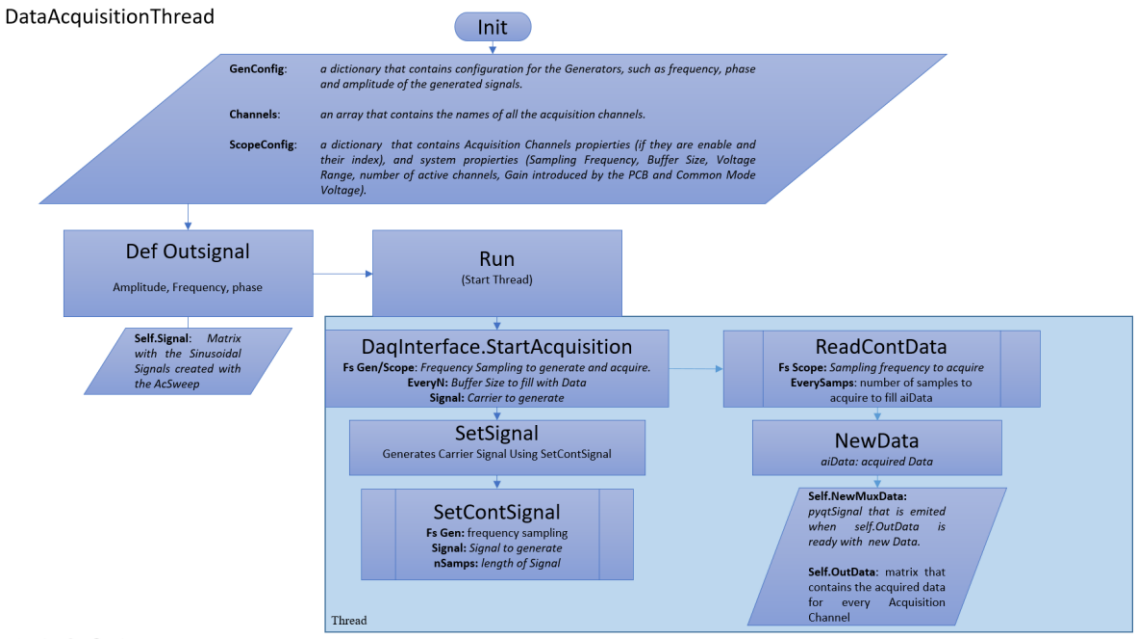

Figure 43 Flowchart of data acquisition thread. Carrier and OL signals are calculated before the process starts. Signal generation and data acquisition start at the same time to ensure synchronization of the system. A signal is emitted when the buffer is filled of acquired data.

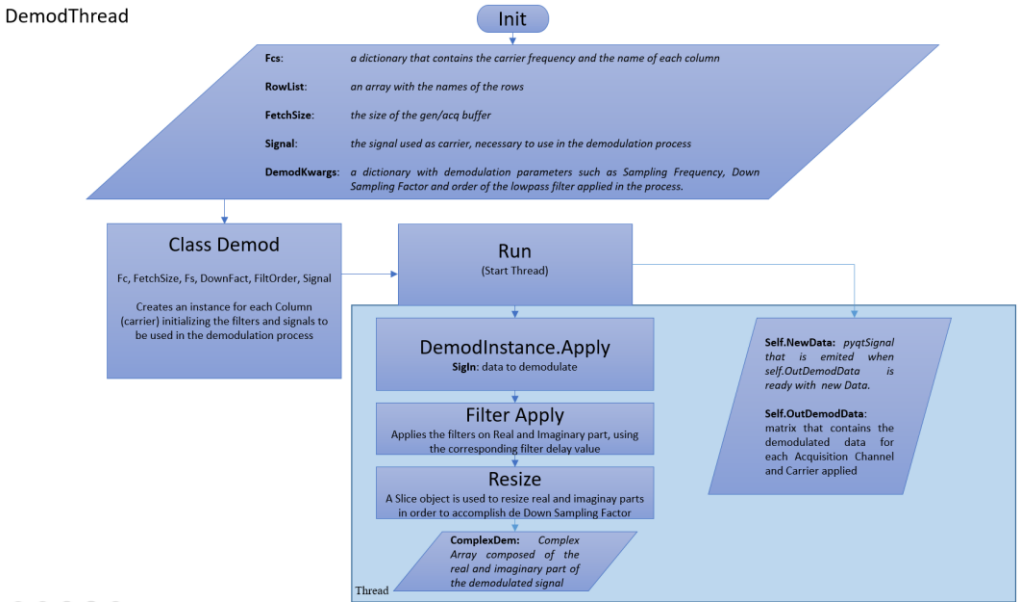

Figure 44 Flowchart of demodulation thread. OL signal is used by the product detector and the demodulated data is resize according to the down sampling factor. A signal is emitted when demodulation process is finished.

The demodulation thread (figure 44) executes a product detector applying a digital low pass filter and down sampling the output to obtain a matrix of demodulated complex data. Finally the stability detector thread (figure 45) calculates the slope of the demodulated data to check if the system is stable, and if so, calculates the power spectral density of the demodulated data and saves DC and AC information used to obtain transistor's parameters such as the transfer curve or its intrinsic noise.

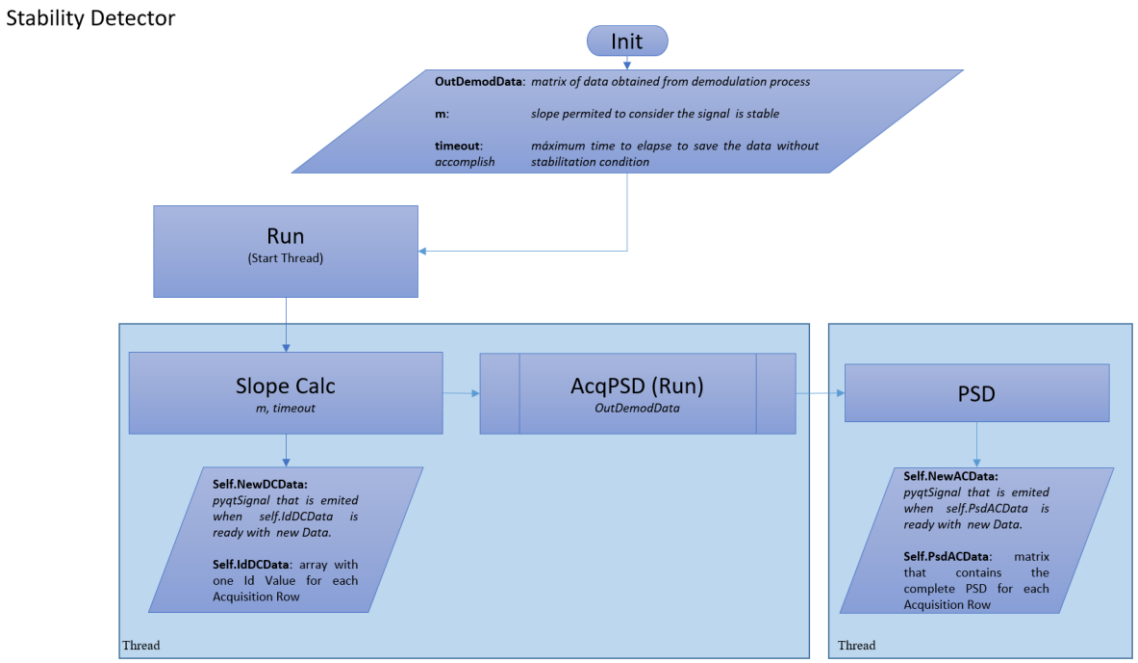

Figure 45 Flowchart of Stability detector thread. Stabilization of the system is checked before proceed to calculate PSD and save DC and AC dictionaries that contain the information to obtain transistor main parameters

5 In-vitro measurements

5.1 AC coupling Test

In-vitro characterization processes have been executed over resistors and transistors arrays with DC and AC coupled systems in order to compare obtained parameters and get information about the behaviour of AC coupled acquisition full system.

5.1.1 Resistor's characterization

Resistors array characterization is useful to check if measured current is proportional to the resistor value applied and ensure there is not attenuation of the signal.

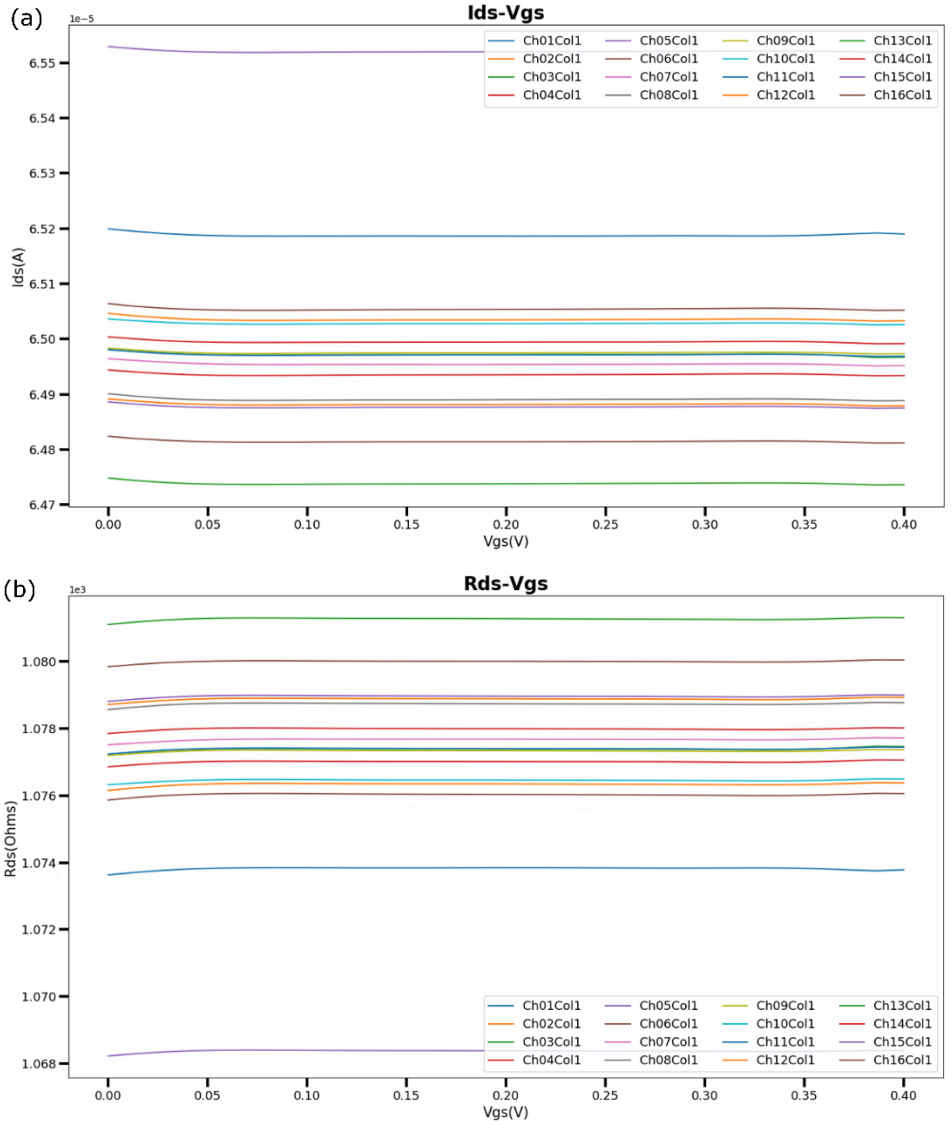

Figure 46 Results obtained from 1kΩ resistors array characterization with V_{ds}=70mV and applying a 30 points sweep of V_{gs} from 0 to 400mV. More stabilization time should be applied at first V_{gs} value to ensure I_{ds} and R_{ds} to be flat.

Ideally channel resistance value of a gSGFET (R_{ds}) is around 1k to 2kΩ, depending on the bias point, so a characterization process has been executed using a 1x16 array of 1kΩ resistors. Considering that drain-to-source applied voltage amplitude is 70mV, expected current values are I_{1ko} = 70µA.

Obtained results (figure 46) show very close current values to these expected and, as a consequence, resistors value given by the system have less than 10% tolerance from the desired value.

5.1.2 Transistor's characterization

Once resistors array characterization has been successful, it is executed the characterization of a 1x16 transistors array also with both systems, DC and AC coupled. Comparing the results of both systems it is possible to determine if transistor's behaviour measured with AC system is as expected.

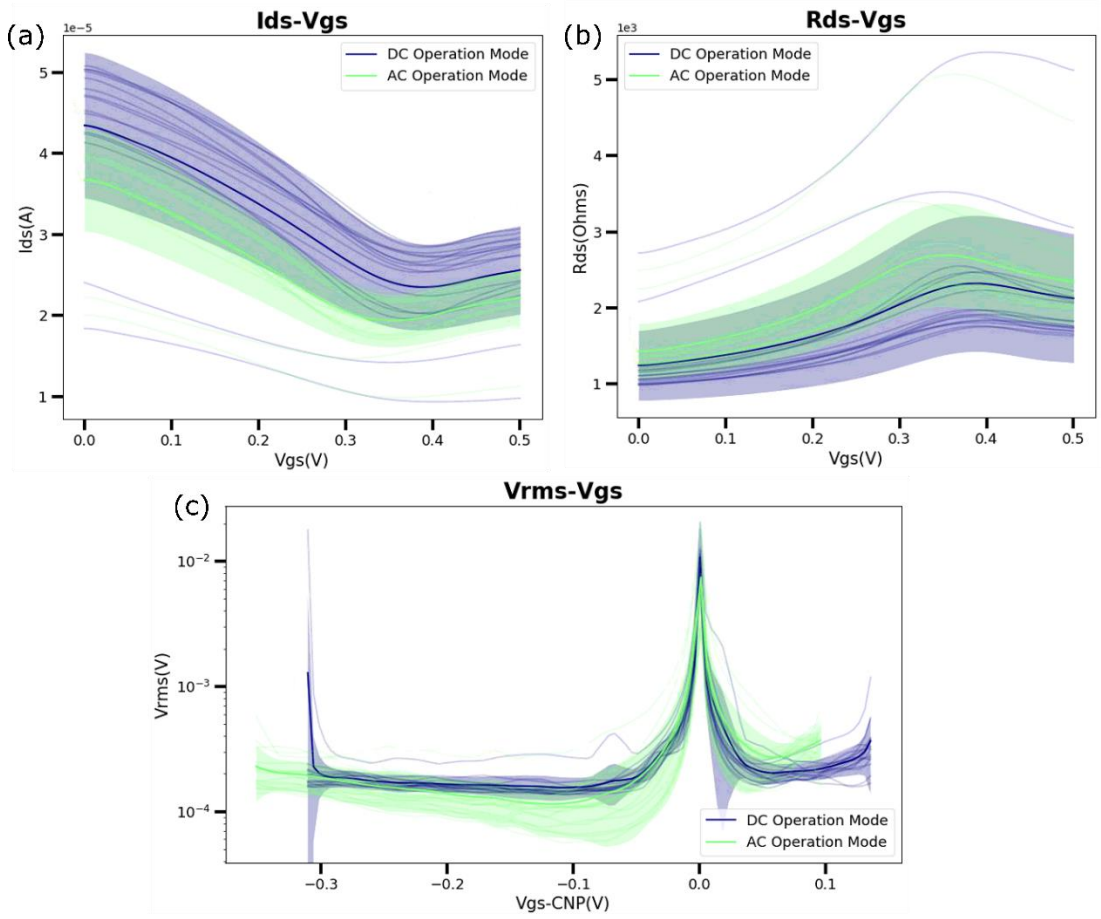

Figure 47 Parameters obtained from the characterization of transistor B13116W2-S4 applying V_{ds}=50mV and a V_{gs} sweep of 30 point from 0V to 500mV. a) b) drain-to-source current (a) and channel resistance R_{ds} (b) obtained with DC (blue) and AC (green) couples systems. c) Noise measured at transistor's gate calculated from the transconducance and the I_{rms} measured at the output signal. X axis is normalized to V_{gs}-CNP.

Main transistor's characteristics to be compare are the transfer curve (figure 47a) and channel resistance (figure 47b) obtained applying a single value of V_{ds}. Results show a maximum difference of 4µA (330Ω) between both systems, being AC coupled the one with bigger R_{ds} values. Also Dirac Point value is different depending on the system used because of the shift that suffers CNP when changing V_{ds} value, that affects DC coupled but not AC coupled system.

Another transitor's characteristic to bear in mind is V_{rms} (figure 47c) that shows the equivalent noise at the gate of the devices calculated from I_{rms} measured and the transconductance of the channel. As it can be seen transistor's noise is reduced in the Dirac Point, showing transcondutance influence on this parameter, and its mean value is around 100µV. Taking into account that mean noise value of a gSGFET is expected to be around 20µV, this transistor array is considered noisy.

5.1.3 Noise characterization

The measurements executed using resistors array permits to obtain electronic noise (figure 48) of DC and AC systems. It can be seen that DC system noise at low frequencies is dominated by electronics flicker noise, nevertheless this noise does not affect AC coupled system because information is carried on the carrier signal whose frequency is much higher than electronics noise frequency.

However, DC coupled system floor noise is lower thanks to the possibility of separate DC and AC signals and amplify only AC ones. This is not possible at AC coupled system whose noise is limited by the resolution, that depends mainly on the number of bits of the analog to digital converter used for signal acquisition, but also on the full scale voltage applied (figure 49). Considering that DAQ card USB-6363 uses 16 bits and the measures have been acquired with a 500mV range, the expected resolution of the system is calculated as follows:

$$Resolution_{AC_{coupled}}(V) = \frac{V_{FS}}{2^{n\_bits}} = \frac{2 \cdot 0.5}{2^{16}} = 15.26\mu V \tag{19}$$

$$Resolution_{AC_{coupled}}(A) = \frac{Resolution_{AC_{coupled}}(V)}{R_G} = \frac{15.26\mu}{5k} = 3.05nA \tag{20}$$

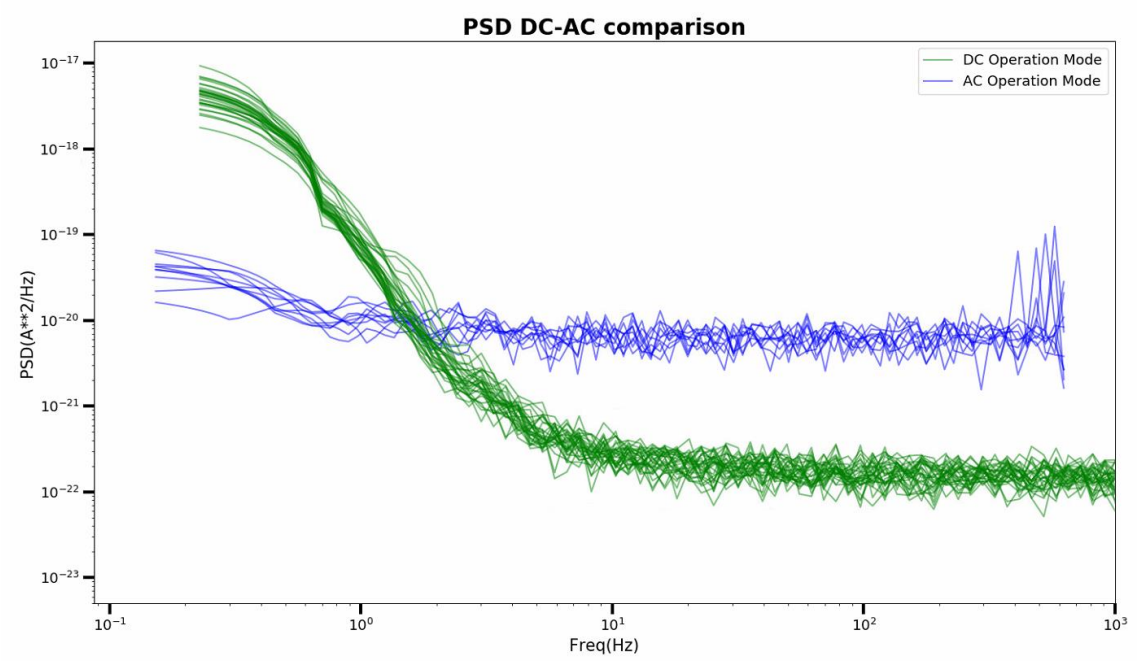

Figure 48 1kΩ resistors array PSD obtained with DC and AC coupled systems. DC coupled system noise (green) is mainly affected by operational amplifiers flicker noise at low frequencies (below 1kHz). AC coupled system has a higher noise (blue) above 1kHz.

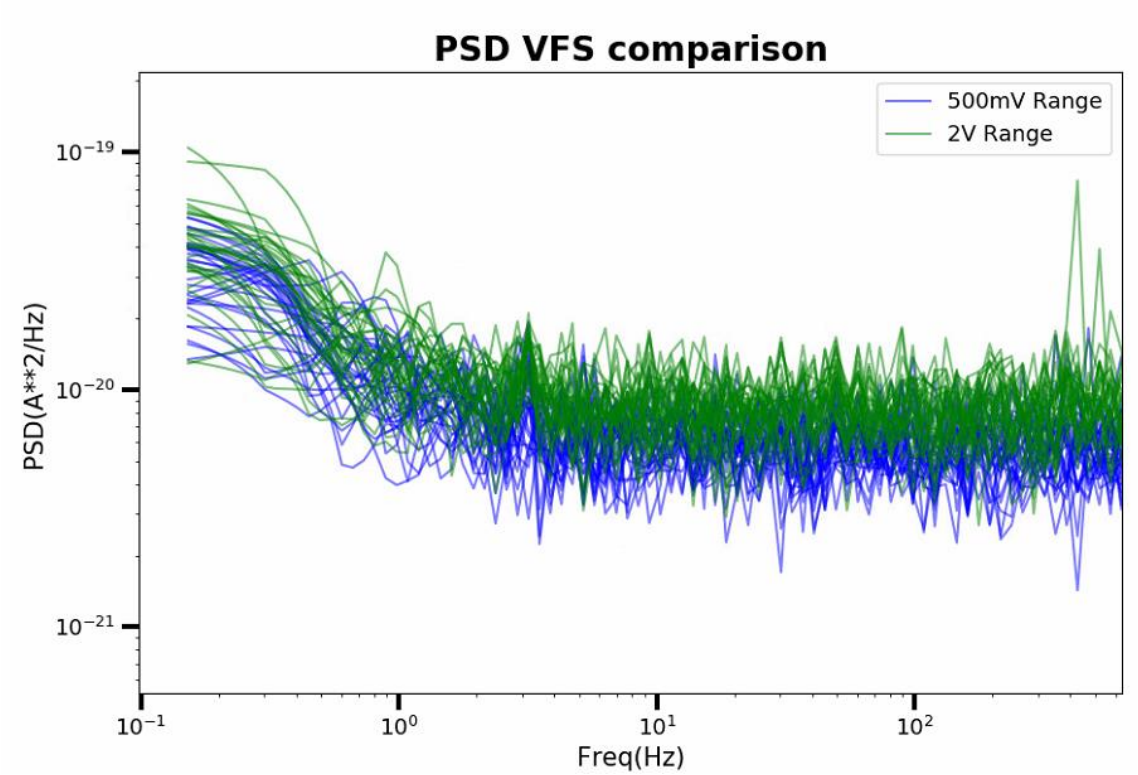

Figure 49 1kΩ resistors array PSD obtained with AC coupled system applying V_{FS}=500mV (blue) and V_{FS}=2V (green). The closer V_{FS} is to V_{carr} maximum voltage the lower the electronic noise measured. To achieve a more noticeable difference an increase on the number of bits used by the ADC is required.

As transistor's noise (figure 50), obtained using AC coupled characterization process, is higher than the electronic floor noise, the minimum voltage amplitude that can be acquired using this system is limited by transistor's noise.

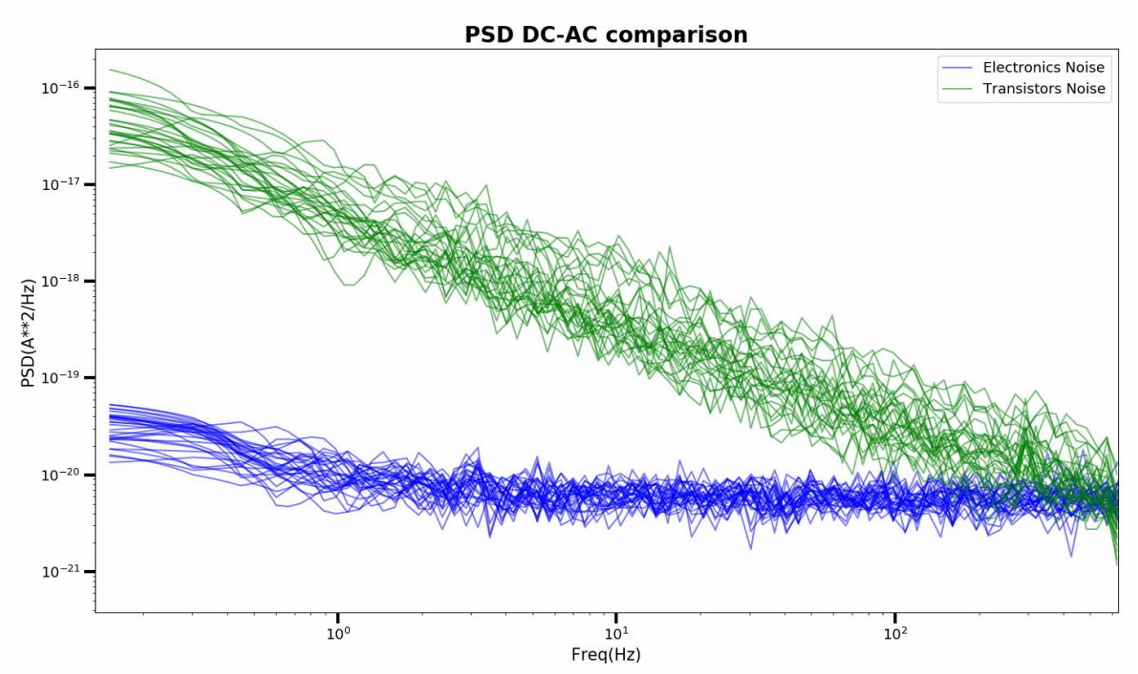

Figure 50 B13116W2-S4 Transistor's noise (Green) is higher than electronic's noise (blue) until 500Hz. The system will be able to recover signals with a frequency below 500Hz and an input voltage higher than 100µV.

5.2 Real Time Acquisition

Finally it is necessary to ensure that AC coupled system is able of acquire, save and recover the signal applied at the gate of the gSGFETs (V_{sig}), for this reason a prove of concept has been done acquiring in real time a sinusoidal signal with 1mV amplitude and a frequency of 10Hz.

Transistors array used for performing the test has been B13116W2-S4, which was also use to check the characterization process using AC coupled system. The carrier signal applied during the measure has a voltage amplitude of $50mV_{rms}$, a frequency of 30kHz and a polarization voltage of 100mV. Also, taking into account that expected R_{ds} values at bias point are between 1kΩ and 2kΩ, dynamic range has been adjusted to 500mV because, for channel resistance worst case, minimum full scale voltage must accomplish:

$$V_{FS} > V_{ds\_peak} \cdot \frac{R_G}{R_{ds}} = V_{ds} \cdot \sqrt{2} \cdot \frac{5k}{1k} \tag{21}$$

$$V_{FS} > 353.55mV$$

To avoid external noise to be induced through connections, wires or voltage and ground plains, all the acquisition system has been introduced in a Faraday cage connected to the same ground of the electronic board.

This way, the frequency spectrum of the modulated signal is shown in figure 51 where it can be seen the signal peak at 30kHz and its first harmonic at 2·30kHz. Also there are several peaks close to carrier frequency due to the harmonics folding and mirroring produced at $F_s/2$ and F_s.

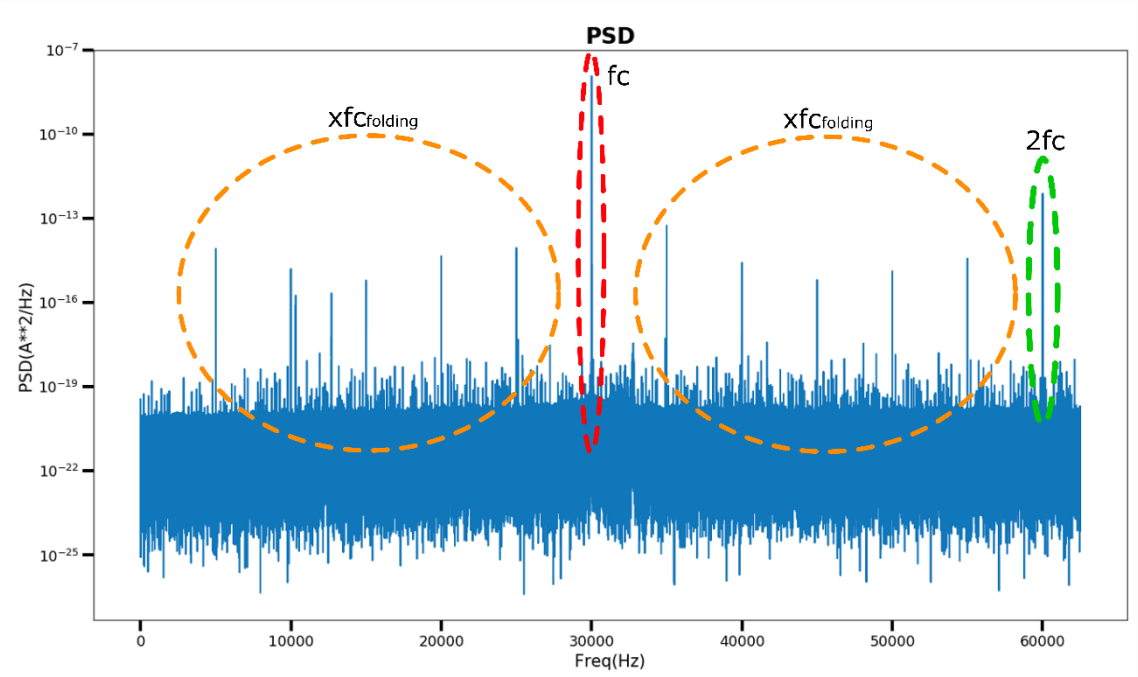

Figure 51 Power spectral density of the acquired data shows a clear carrier peak at 30kHz (red circle) followed by its first harmonic at 60kHz (green circle). Also there are several peaks around the carrier tone due to harmonics folding produced by the sampling frequency. Very low floor noise can be also seen.

To ensure that modulator signal (V_{sig}) can be recovered, its frequency must be lower than the bandwidth available between the carrier signal and the closest harmonic peaks (eq. 22-23). So, if frequency spectrum is zoomed (figure 52) close to the carrier frequency (30kHz) can be perfectly seen the AM modulated signal produced by V_{sig} that introduces two peaks at 30kHz+10Hz y 30kHz-10Hz.

$$f_{H2} = 3 \cdot 30kHz = 90kHz$$

$$f_{H4\_folding} = 2\frac{F_s}{2} - f_{H2} = 125k - 90k = 35kHz \quad (22)$$

$$f_{H4} = 5 \cdot 30kHz = 150kHz$$

$$f_{H4\_mirror} = f_{H4} - F_s = 150k - 125k = 25kHz \quad (23)$$

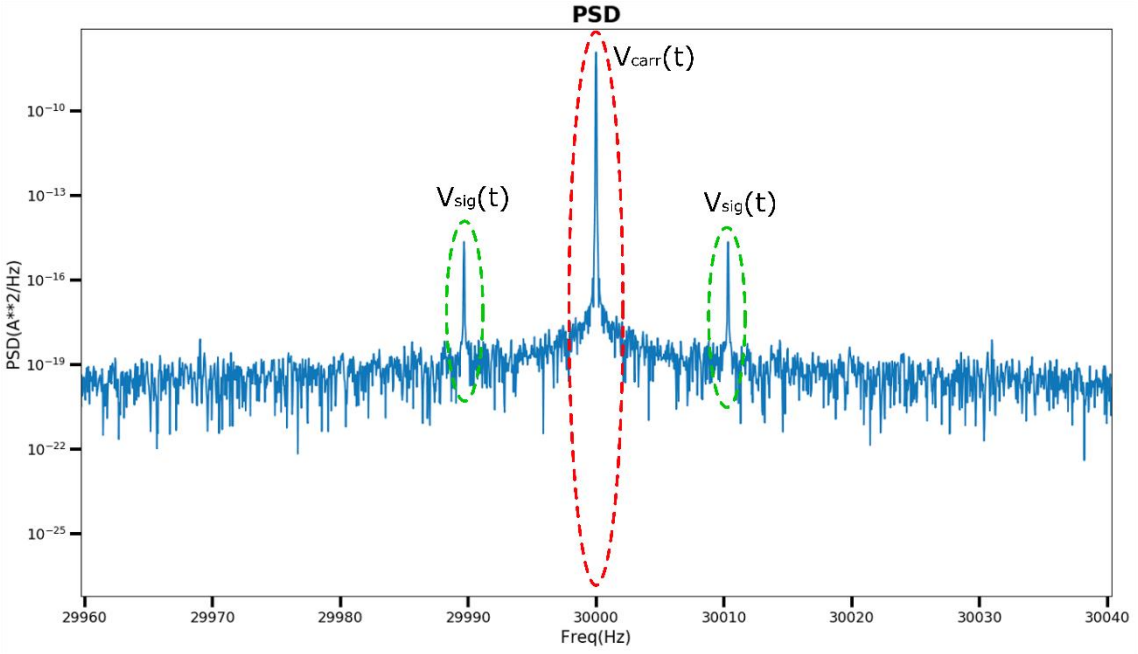

Figure 52 Power spectral density zoom shows the AM modulation of the carrier (red circle) and the modulation signal (green circle). Neither noise nor harmonics are appreciated so demodulation process will be able of recover $V_{sig}(t)$.

Due to the fact that the recorded signal $V_{sig}(t)$ is acquired as a variation of the transistor's channel current (I_{ds}) following the expression in equation 24, it is need to know transconductance (g_m) value to recover correctly signal amplitude.:

$$I_{ds} = V_{carr}(t) \cdot \left(G_{ds-DC} + g_m V_{sig}(t)\right) \quad (24)$$

Because of transfer curve's differences between transistors of the same array, an interpolation with the recorded signal (figure 53) is executed in order to know the exact V_{gs} for each value of I measured, thus reducing the error produced by the non-linearity of the transconductance.

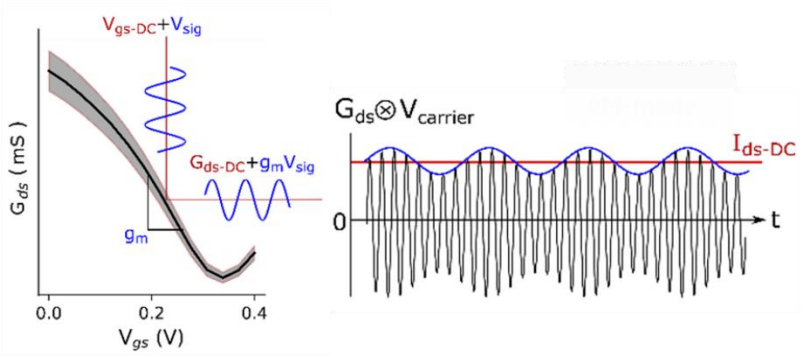

Figure 53 DC current measured ($I_{ds\text{-}DC}$) indicates in which point of the transfer curve has been polarized the transistor, providing the transconductance (g_m) value need to recover $V_{sig}(t)$ amplitude.

After applying the calibration process to the data obtained using real time measurement of AC coupled system, 1mV signal is recovered with its 10Hz frequency (figures 54, 55) showing 10 cycles in 1 second of plot. Also it can be appreciated that recovered signals have an offset with a value close to 100mV, this is because continuous voltage from biasing transistors (V_{DC}) is maintained despite of being an AC coupled system. To remove this offset voltage a high pass digital filter with a cut-off frequency of 0.1Hz can be applied to the recovered signal obtaining the same result but centred at 0V (figure 56).

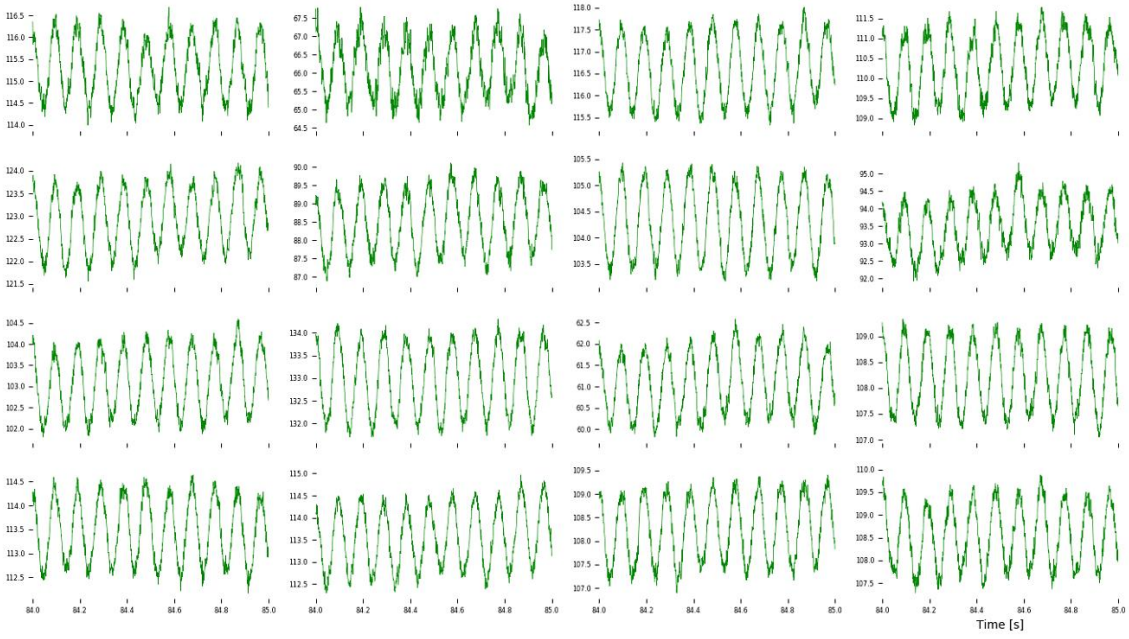

Figure 54 $V_{sig}(t)$ measured with AC coupled system. Signal frequency and amplitude are recovered and it can be seen the offset introduced by the bias voltage applied. Not all the offset voltages are the same due to the differences in the transfer curves between devices.

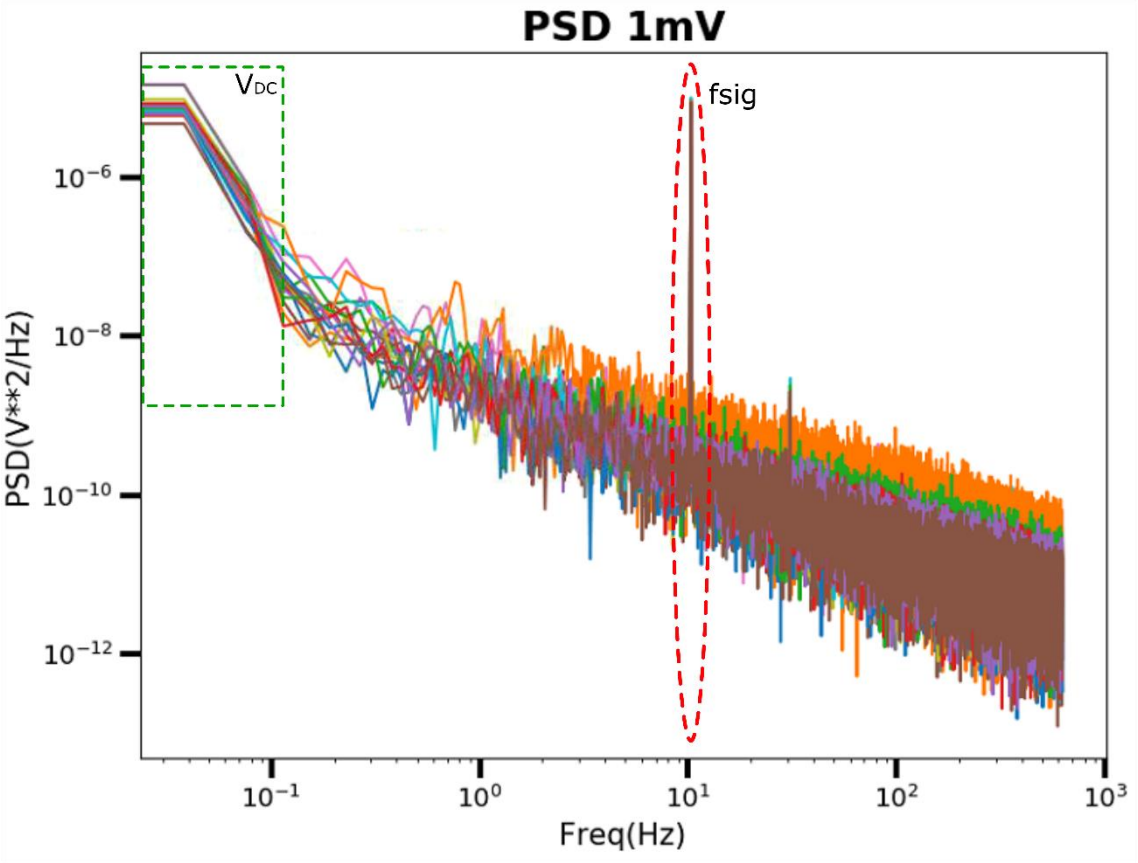

Figure 55 The power spectral density of the demodulated signal shows the peak corresponding to bias voltage (green square) and the tone of the recovered signal of 10Hz (red circle)

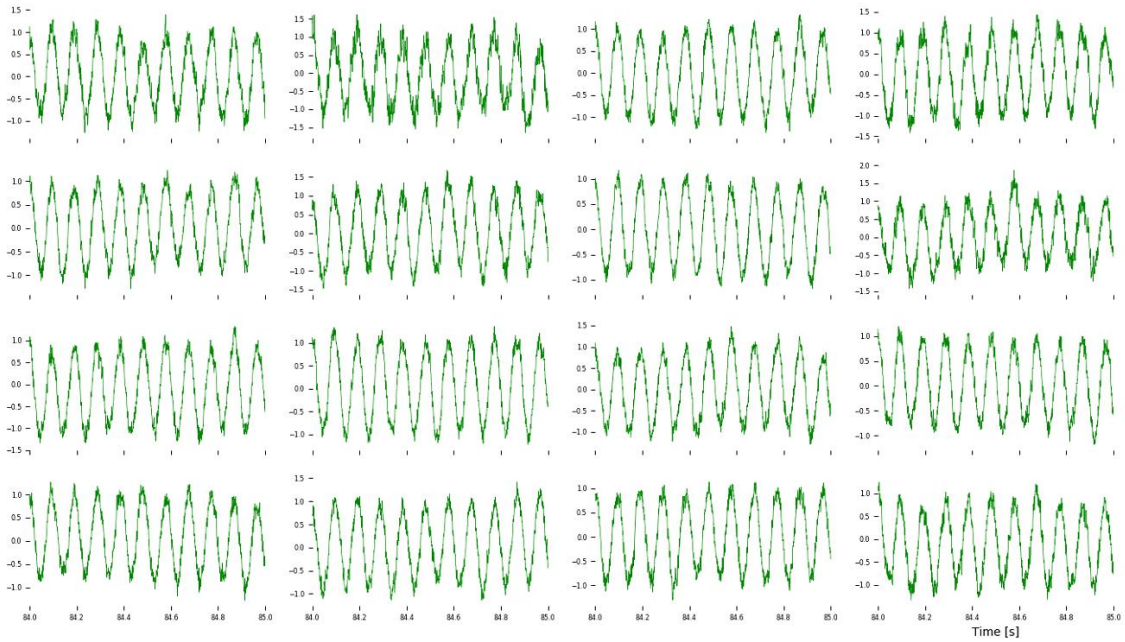

Figure 56 Applying a high pass filter with fc=0.1Hz the DC voltage from biasing transistors is remover so the recovered signal does not show any offset.

As shown, transistor's noise is bigger than electronics intrinsic noise, which means that it limits the minimum voltage the system is able to recover. To demonstrate this assertion, a real-time recording using AC coupled system has been performed introducing, as gate signal, a pure tone with 10Hz frequency and 100µV amplitude.

Due to the fact that transistors array B13116W2-S4 mean noise is around 100µV, the signal obtained after calibration process (figure 57) is a mixture of noise and gate signal where frequency and amplitude can't be appreciated. On the other hand, frequency spectrum (figure 58) clearly shows the 10Hz frequency peak so the signal could be recovered by applying a digital and narrow band pass filter around the desired peak.

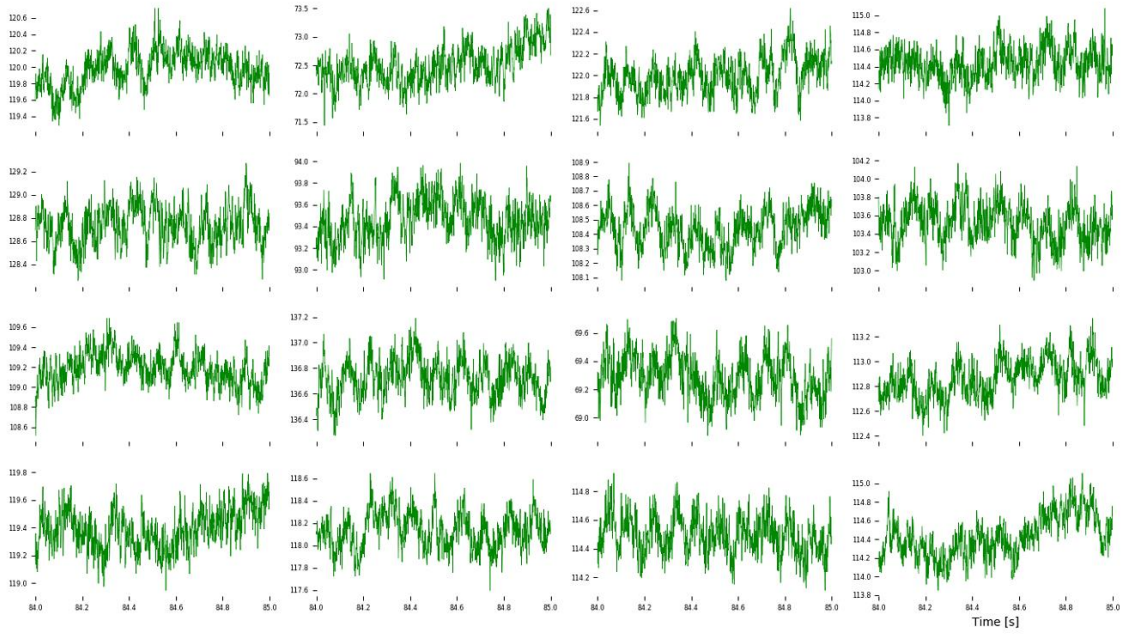

Figure 57 $V_{sig}(t)$ measured with AC coupled system. As signal amplitude introduced is around 100µV, same value as transistor's intrinsic noise, the system is unable to recover the signal.

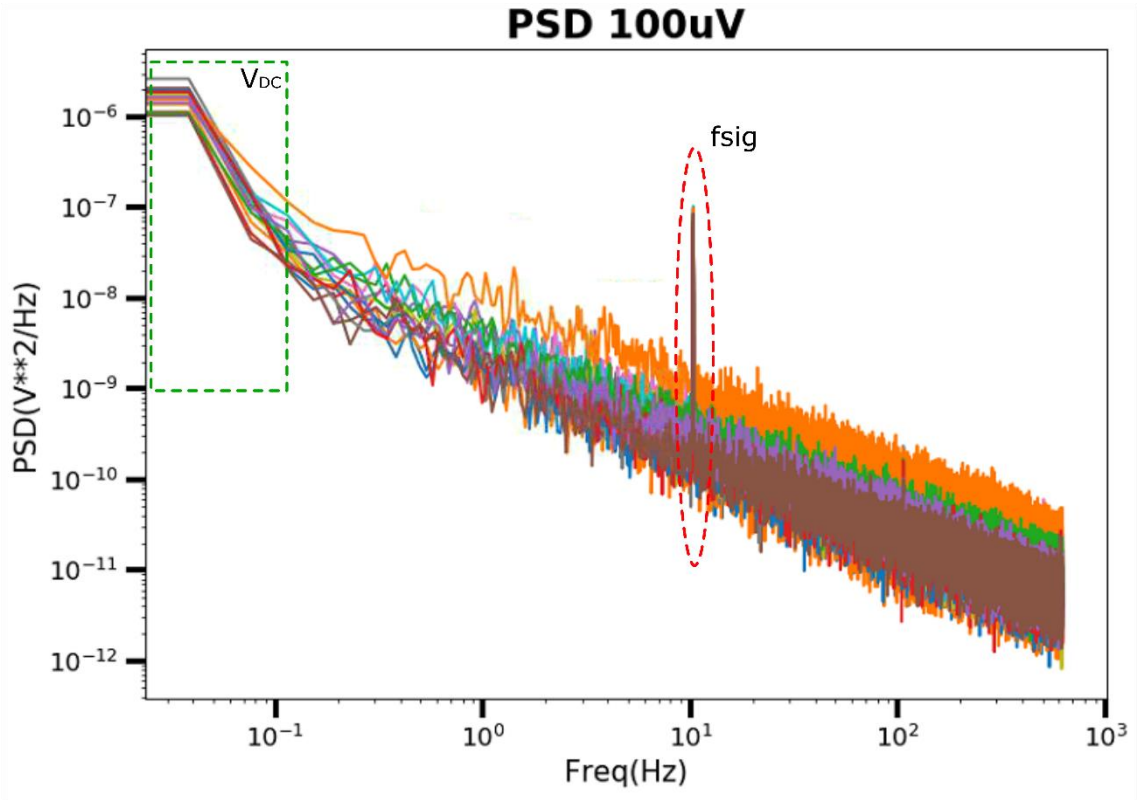

Figure 58 although the signal can't be appreciated in temporary domain, power spectral density clearly shows the signal tone at 10Hz frequency, which means that applying a narrow band pass filter by software, the signal can be recovered.

6 Conclusions

The main conclusions of this Master Thesis can be summarized as follows:

- The electrical safety regulatory applicable to gSGFET acquisition system has been evaluated.
- An AC coupled electronic system, able to acquire neural signals using gSGFET array, has been designed and developed accomplishing safety regulatory.
- The effect of protection elements in the system behaviour and recovered signal has been studied.
- Electronic noise has been optimized to achieve the recording of low amplitude signals.
- gSGFETs characterization process has been validated using the AC coupled system.
- gSGFETs real time recording performance has been validated using AC coupled system and test signals.

The aforementioned achievements have allowed to accomplish the main goal of this Master Thesis since the obtained results shows the capability of the system to record and recover low voltage signals applied at the gate of gSGFET transistors while accomplishing IEC60601-1 regulation.

It is worth to mention that the system designed is not affected by electronic flicker noise. However, the floor noise of the acquisition system presented is limited by the analog to digital converter used. An ADC with a higher number of bits should be implemented to ensure electronic noise to be lower than transistor's noise.

Summarizing, this Master Thesis introduces a system design able to record and recover low frequency and amplitude signals accomplishing electrical regulations for medical equipment, bringing a way to implement gSGFETs array recordings in human clinical trials.

Acknowledgments

During the development of this Master Thesis I had the opportunity to widen my knowledge about semiconductors, electronic design and software programming. I want to thank all the people who helped me to achieve the main objective of this work. Firstly, I want to thank the whole Biomedical Applications Group their great reception, help and companionship during each workday. Especially to Dra. Rosa Villa to have given me the opportunity to start working in the group and develop this Master Thesis based on my everyday work; and to my director Dr. Anton Guimerà for helping me to better understand and assimilate concepts about semiconductors physics, signals treatment and electronics, and learning a new programming language. Secondly, to my office mates, Eduard Masvidal for providing me transistor arrays I could use to carry out acquisition system tests, and for the explanations about how to perform data processing and understand the obtained information; and to Javier Martinez for the talks in the office, the explanations given about IMB-CNM methods when I arrived, and for try to help me with PCB's and software problems or doubts.

I would like to also thanks to Prof. Jose Antonio Garrido and his full AEMD group for every week meetings where I could learn about other areas related to graphene devices; especially to Ramon Garcia for giving me knowledge about non-idealities and frequency multiplexing strategies. Also I want to mention Dr. Francesc Serra and Jose Cisneros for the meetings to discuss about results obtained from tests and define improvements in the acquisition system's electronic design.

Finally, I want to say thanks to my family, my parents Mariana and Osbel and my sister Ariadna, for their unconditional support and be always encouraging me to keep going. And to Ivan for his support and patience in day to day, and his contribution to finish this work in time.

Referencias

[1] R. Fohlmann Andersen, H. Carlsson Kamban and R. & Lau Riksted, *Study of the pi and pi* Electronic Bands in Graphene,* Institue of Physics and Nanotechnology Aalborg University, 2015.

[2] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov and A. K. & Geim, "The electronic properties of graphene," *Reviews of Modern Physics,* p. 10.1103/RevModPhys.81.109, 2009.

[3] M. J. Rogoff and S. & Francois, "Chapter 3 - WTE technology," in *Waste-to-Energy (Second Edition) Technologies and Project Implementation*, William Andrew, 2011, pp. 21-43.

[4] G. Brunner, "Chapter 10 - Oxidation in High-Temperature and Supercritial Water," in *Supercritical Fluid Science and Technology, Volume 5*, ELSEVIER, 2014, pp. 525-568.

[5] M. Kalbacova, A. Broz, J. Kong and M. & Kalbac, "Graphene substrates promote adherence of human osteoblasts and mesenchymal stromal cells," *Carbon, 48(15), 4323-4329,* p. 10.1016/j.carbon.2010.07.045, 2010.

[6] D. A. C. Brownson, S. A. Varey, F. Hussain, S. J. Haigh and C. E. & Banks, "Electrochemical properties of CVD grown pristine graphene: monolayer- vs. quasi-graphene," *Nanoscale, 2014, 6, 1607,* p. DOI: 10.1039/c3nr05643k.

[7] J. -W. Jeong, G. Shin, S. I. Park, K. J. YU, L. Xu and J. A. & Rogers, "Soft Materials in Neuroengineering for Hard Problems in Neuroscience," *Neuron, 86(1), 175-186,* p. https://doi.org/10.1016/j.neuron.2014.12.035, 2014.

[8] R. R. Nair, P. Blake, A. N. Grigorenko, K. S. Novoselov, T. J. Booth, T. Stauber and A. K. & Geim, "Fine structure constant defines visual transparency of graphene," *Science, 320(5881), 1308-1308,* p. 10.1126/science.1156965, 2008.

[9] P. Bergveld, «Development of an Ion-Sensitive Solid-State Device for Neurophysiological Measurements,» *IEEE Transactions on Biomedical Engineering, BME-17(1), 70-71,* p. 10.1109/TBME.1970.4502688, 1970.

[10] C. Hébert, E. Masvidal-Codina, A. Suarez-Perez, A. Bonaccini Calia, G. Piret, R. Garcia-Cortadella and J. A. ... Garrido, "Flexible Graphene Solution-Gated Field-Effect Transistors: Efficient Transducers for Micro-Electrocorticogaphy," *Advanced Functional Materials, 28(12), 1703976,* p. 10.1002/adfm.201703976, 2017.

[11] N. Schaefer, R. Garcia-Cortadella, J. Martinez-Aguilar, G. Schwesig, X. Illa, A. Moya Lara and J. A. ... Garrido, "Multiplexed neural sensor array of graphene solution-gated field-

effect transistors," *2D Materials, 7,* pp. https://doi.org/10.1088/2053-1583/ab7976, 2020.

[12] M. E. J. Obien, K. Deligkaris, T. Bullmann, D. J. .. Bakkum and U. & Frey, "Revealing neuronal function through microelectrode array recordings," *Frontiers in Neuroscience, 8,* p. https://doi.org/10.3389/fnins.2014.00423, 2015.

[13] E. Masvidal Codina, "Modelling and fabrication of graphene solution-gated field-effect transistors for electrophysiological applications," Master in Advanced Nanoscience and Nanotechonology - Universitat Autònoma de Barcelona, 2016.

[14] E. V. Rut'kov, E. Y. Afanas'eva and N. & Gail, "Graphene and graphite work function depending on layer number of Re," *Diamond and related materials, 101,* p. https://doi.org/10.1016/j.diamond.2019.107576, 2020.

[15] M. S. Simon and K. N. & Kwok, Physics of Semicnductor Devices, Wiley, 1969.

[16] M. e. e. -. P. 1. G. r. f. b. s. a. e. performance, "International Standard - IEC 60601-1," 2005. [Online]. Available: https://www.ele.uri.edu/courses/bme484/iec60601-1ed3.0_parts.pdf.

[17] R. L. E. Llamosa, L. G. Meza Conteras and H. & Parra Lara, "Fundamentos para el diseño de la prueba de seguridad electrica para equipo biomedico con base en la norma NTC-ISO-IEC-60601-1," *Scientia Et Technia, 12(30), 321-326,* 2006.

[18] R. Garcia-Cortadella, N. Schaefer, J. Cisneros, L. Re, X. Illa, G. Schwesig and A. ... Guimerà-Brunet, "Switchless Multiplexing of Graphene Active Sensor Arrays for Brain Mapping," *Nano Lett. 2020, 20, 5, 3528-3537,* p. 10.1021/acs.nanolett.0c00467, 2020.

[19] E. Masvidal-Codina, x. Illa, M. Dasliva, A. B. Calia, T. Dragojevic, E. E. Vidal-Rosas and A. ... Guimerà-Brunet, "High-resolution mapping of infraslow cortical brain activity enabled by graphene microntrasistors.," *Nature Materials, 18(3), 280-288,* pp. 10.1038/s41563-018-0249-4, 2018.

[20] M. Olmo and R. & Nave, "HyperPhysics - Electricidad y Magnetismo," [Online]. Available: http://hyperphysics.phy-astr.gsu.edu/hbasees/electric/capchg.html.

[21] R. Garcia-Cortadella, E. Masvidal-Codina, J. M. De la Cruz, N. Chaefer, G. Schwesig, C. Jeschke and J. A. ... Garrido, "Distortion-Free Sensing of Neural Activity Using Graphene Transistors," *Nano-micro small, 16(16), 1906640,* p. 10.1002/smll.201906640, 2020.

[22] K. A. Jenkins, D. B. Farmer, S.-J. D. C. Han, S. Oida and A. & Valdes-Garcia, "Linearity of graphene field-effect transistors," *Appl. Phys. Lett. 103, 173115,* p. 10.1063/1.4826932, 2013.

[23] S. Drieschner, A. Guimera, R. Garcia-Cortadella, D. Viana, E. Makrygiannis, B. M Blaschke, J. Vieten and J. A. and Garrido, "Frequency response of electrolyte-gated graphene

electrodes and transistors," *J. Phys. D: Appl. Phys. 50 095304,* pp. 10.1088/1361-6463/aa5443, 2017.

[24] M. Guibord, "Digital-to-Analog Converter (DAC) Output Response - TIPL 4705," Texas Instruments.

[25] L. Re, "Branch: SweepFreqDaq fromo Code: Pyxi," aguimera, [Online]. Available: https://github.com/aguimera/Pyxi/tree/SweepFreqDaq.

[26] 2xB, "Branch: master from Code: pyqtgraph," pyqtgraph, [Online]. Available: https://github.com/pyqtgraph/pyqtgraph/tree/master/pyqtgraph/parametertree.